



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

SERIAL NO.: 10/817,140

RCE FILED: October 25, 2007

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK

§ GROUP ART UNIT: 1756

§ (In parent case)

§

§ EXAMINER: B.L. Raymond

§ (In parent case)

§

§

§ Attorney Docket No.:

§ AM-8893 Y1

Date: February 25, 2008

**RESPONSE TO DECISION ON PETITION IN SUPPORT OF  
DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131  
TRANSMITTAL LETTER**


**Mail Stop PETITION  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450**

Transmitted herewith is applicants' Response to Decision Dismissing Petition, including Exhibit "A" - Declaration of Line Gauthier Under MPEP 409.03(d); Exhibit "B" - internet search results; Exhibit "C" - letter and accompanying documents sent to Inventor Stephen Osborne requesting signature; Exhibit "D" - statement from U.S. Post Office Delivery personnel; and a copy of the Declaration of Prior Invention Under 37 CFR § 1.131 with Inventor Homer Lem's signature. For reference purposes, applicants have also enclosed a copy of the Petition in

**CERTIFICATE OF MAILING UNDER 37 CFR § 1.10**

I hereby certify that this paper is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as U.S. EXPRESS MAIL NO. EB 998981707 US in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: February 25, 2008

  
Shirley L. Church, Reg. No. 31,858

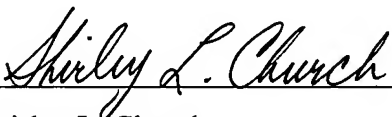
Support of Declaration of Prior Invention Under 37 CFR§ 1.131 including a copy of the original Invention Alert signed by all five of the inventors.

Applicants do not believe that any additional fee is due in connection with the filing of this Response to Decision Dismissing Petition. However, in the event any fees are due, the Commissioner is hereby authorized to charge any additional fees which may be due, and to credit any overpayment to Deposit Account No. 50-1512 of Shirley L. Church, Esq. of San Diego, California, in the amount of such fee.

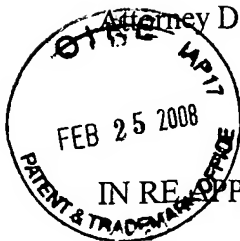
This transmittal letter is submitted in duplicate for accounting purposes.

Respectfully Submitted,

Date: February 25, 2008

  
\_\_\_\_\_  
Shirley L. Church  
Registration No. 31,858  
Attorney for Applicants  
(858) 587-6633

Correspondence Address:  
Shirley L. Church, Esq.  
P.O. Box 81146  
San Diego, CA 92138

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**RESPONSE TO DECISION ON PETITION IN SUPPORT OF  
DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131  
TRANSMITTAL LETTER****Mail Stop PETITION  
Commissioner for Patents  
P.O. Box 1450  
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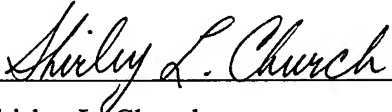
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This transmittal letter is submitted in duplicate for accounting purposes.

Respectfully Submitted,

Date: February 25, 2008

  
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Shirley L. Church  
Registration No. 31,858  
Attorney for Applicants  
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§ EXAMINER: B.L. Raymond

§ (In parent case)

§

§

§ Attorney Docket No.:

§ AM-8893 Y1

Date: February 25, 2008

**RESPONSE TO DECISION DISMISSING PETITION MAILED JANUARY 3, 2008**

**Mail Stop PETITION**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, VA 22313-1450**

Sir:

1. This Response to Decision Dismissing Petition is in reply to the Decision on Petition mailed January 3, 2008.
2. This Response is made to obtain acceptance of the Petition In Support of Declaration of Prior Invention Under 37 CFR § 1.131. The Petition accompanied Response "B", which was made in reply to the Office Action mailed July 25, 2007. Petition Attorney Grant informed applicants' attorney in her Decision On Petition, that the Petition was dismissed because the

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**CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

I hereby certify that this paper and any documents said to accompany this paper are being deposited with the U.S. Postal Service on the date shown below with sufficient postage as U.S. EXPRESS MAIL NO. EB 998981707 US in an envelope addressed to : Mail Stop PETITION, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: February 25, 2008

  
Shirley L. Church, Reg. No. 31,858

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Petition Examiner concluded that Petitioner had failed to show adequate proof that a diligent effort was made to reach or locate inventors Osborne and Lem.

3. Applicants' attorney, with the exercise of diligent effort, has located inventor Homer Lem who has signed the Declaration Of Prior Invention Under 37 CFR § 1.131. Applicants are enclosing a copy of the Declaration executed by inventor Lem.

4. Applicants have now found four of the five inventors, each of whom has signed the Declaration Of Prior Invention Under 37 CFR § 1.131.

5. On January 17, 2008, an assistant of applicant's attorney, Line Gauthier, searched for information regarding the fifth inventor, Stephen Osborne. Inventor Osborne no longer works for Applied Materials, Inc. and left without giving a forwarding address to his employer. Applicants used the Internet search engines Google and [www.peoplelookup.com](http://www.peoplelookup.com) and found numerous persons named Stephen Osborne scattered across the United States. Applicants telephoned the Phone Operator asking for phone numbers relating to the name Stephen Osborne in the city where Inventor Osborne was last known to reside, Hayward, California, and its vicinity. The Phone Operator offered three phone numbers, which applicants dialed. All three phone numbers were wrong numbers.

6. Further, on January 17, 2008, applicants sent a letter to Inventor Osborne at his last known address, via Express Mail, requesting a delivery signature, and including a request letter, the Declaration of Prior Invention Under 37 CFR § 1.131, the Invention Alert Form, a copy of the application as filed, and a self-addressed, stamped envelope.

7. On February 6, 2008, the U.S. Postal Service returned the unopened package to applicants' attorney stating that Stephen Osborne had moved leaving no forwarding address.

8. On February 12, 2008, we extended our research outside of the Hayward area and requested assistance from the Phone Operator to find a Stephen P. Osborne in Woodland Hills, California; Middleton, Wisconsin; Santa Monica, California; and Santa Clara, California. There were no such listings.

9. Applicants are enclosing a copy of the internet search results (Exhibit "B"), a copy of the letter to Inventor Osborne and accompanying documents (Exhibit "C"), and a copy of the returned envelope with the U.S. Postal Service statement that Inventor Osborne moved without leaving a forwarding address (Exhibit "D").

10. Applicants believe that the enclosed documents are adequate proof that a diligent effort was made to locate Inventor Osborne, who left his place of employment and residence without leaving a forwarding address either to his employer or with the U.S. Postal Services. A Statement Of Facts that fully describes the exact facts which applicants are relying upon to establish that a diligent effort was made to locate Inventor Osborne is also enclosed (Exhibit "A"). The Statement is signed by attorney's assistant, Line Gauthier, who performed the research and prepared the letter sent to Inventor Osborne, and who, thus, has first hand knowledge of the facts recited therein.

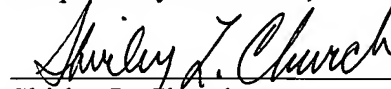
11. Applicants have obtained the signatures of four of the five inventors on the Declaration of Prior Invention Under 37 CFR § 1.131; combined with this is the fact that all five of the inventors executed an Invention Alert describing the invention prior to the date at issue (and a copy of that Invention Alert has been submitted as part of the Declaration of Prior Invention). The Office of Petitions is respectfully requested to grant the Petition In Support of Declaration of Prior Invention Under 37 CFR § 1.131 in Application Serial No. 10/817,140. This Petition requests the Declaration of Prior Invention Under 37 CFR § 1.131 be accepted without the signature of one inventor (Stephen Osborne). Granting of the Petition is necessary so that

inventors' Declaration of Prior Invention will be accepted by Examiner B.L. Raymond in pending Application Serial No. 10/817,140.

12. This Petition is accompanied by the fee required under 37 CFR § 1.17(f).

Date: February 25, 2008

Respectfully submitted,

A handwritten signature in cursive script, reading "Shirley L. Church", is written over a horizontal line.

Shirley L. Church

Registration No. 31,858

Attorney for Applicants

(858) 587-6633

Correspondence Address:

Customer No. 60767

Shirley L. Church, Esq.

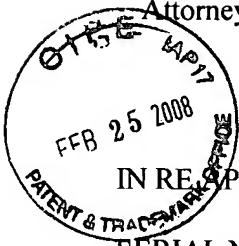
P.O. Box 81146

San Diego, California 92138



Attorney Docket No.: AM-8893 Y1

U.S. Express Mail No. EB 998981707 US



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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SERIAL NO.: 10/817,140

FILED: April 2, 2004

FOR: METHOD OF IMPROVING THE UNIFORMITY  
OF A PATTERNED RESIST ON A PHOTOMASK

§ GROUP ART UNIT: 1763

§

§

§ EXAMINER: B.L. Raymond

§

§

§ ATTORNEY DOCKET NO.:  
AM-8893 Y1

Date: February 25, 2008

**DECLARATION OF LINE GAUTHIER UNDER MPEP 409.03(d)**  
**EXHIBIT "A"**

**Mail Stop PETITION**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, Virginia 22313-1450**

This Declaration under MPEP 409.03(d) accompanies a response to the Decision Dismissing Petition mailed January 3, 2008.

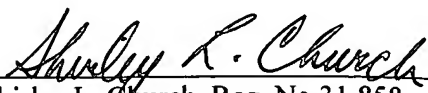
I, Line Gauthier, an assistant to Shirley L. Church, Esq., having firsthand knowledge of the facts recited herein, declare that the statements below are the exact facts showing the diligent effort I exercised to locate Inventor Stephen P. Osborne, an inventor of the invention claimed in U.S. Patent Application Serial No. 10/817,140, who no longer works for Applied Materials, Inc. and who has left no forwarding address with his last known employer, Applied Materials, Inc. nor with the U.S. Postal Services at his last known address.

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Date: February 25, 2008

  
Shirley L. Church, Reg. No. 31,858

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1. Inventor Osborne's last known address is 1128 "D" Street, Hayward, CA 94541.
2. On January 17, 2008, I searched the name Stephen Osborne in the Google search engine and found [www.peoplelookup.com](http://www.peoplelookup.com), which listed a large number of Stephen P. Osborne in several cities, in several states, thus rendering the search difficult. A copy of the search result is enclosed (Exhibit "B").
3. I called the Phone Operator and asked if a phone number was available for a Stephen P. Osborne in Hayward or near Hayward, California. The operator had only one listed number for Stephen P. Osborne in Hayward and two more in Santa Clara and Valencia. I called the number in Hayward but was told this was the wrong Stephen Osborne.
4. I called the other two phone numbers in Santa Clara and Valencia and was told they were wrong numbers.
5. In order to extend the scope of my search, I called the Phone Operator for assistance in finding listings for Stephen P. Osborne in Canyon Country, California; Woodland Hills, California; Middleton, Wisconsin; Santa Monica, California; and Santa Clara, California. There were no such listings.
6. On January 17, 2008, I sent a letter to Mr. Osborne at his last known address, via Express Mail, requesting a signature at delivery. Copies of the letter, the Declaration of Prior Invention Under 37 CFR § 1.131, the Invention Alert Form and application as filed are enclosed, self-addressed, stamped return envelope are enclosed (Exhibit "C").
7. On February 6, 2008, the United States Post Service returned the package to us indicating that Stephen Osborne had moved without leaving a forwarding address. A copy of the returned envelope showing the statement from the U.S. Post Service delivery person is also enclosed (Exhibit "D").

8. On February 12, 2008, I extended my research outside of the Hayward area and requested assistance from the Phone Operator to find a Stephen P. Osborne in Woodland Hills, California; Middleton, Wisconsin; Santa Monica, California; and Santa Clara, California. There were no such listings.
9. I have no telephone number for Stephen P. Osborne and no current address after having made the above-described effort to locate Stephen P. Osborne.

2/14/2008  
Date:

Line Gauthier  
Line Gauthier

Attorney Docket No. AM-8893 Y1

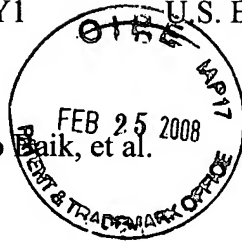
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§ GROUP ART UNIT: 1763

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§  
§ EXAMINER: B.L. Raymond

§  
§ ATTORNEY DOCKET NO.:  
§ AM-8893 Y1

**EXHIBIT "B"**

**WWW.PEOPLELOOKUP.COM SEARCH RESULTS**



People Search

Reverse Phone

Background Check

Cell Phone ID

Other Services

Login | My Account

Customer Service

PEOPLE LOOKUP RESULTS

41 People found that match Stephen Osborne .  
Click on the Name or View Details link for more info.  
✓ = Available Information

Search Again >>

See Details on All 41 People!

	NAME	AGE	PREVIOUS CITIES	DOB	PHONE	ADDRESS	RELATIVES
1	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	39	PAHRUMP, NV YUMA, AZ TUCSON, AZ	✓	✓	✓	STEVE P OSBORNE VIRGINIA C OSBORNE MARK W OSBORNE WILLIAM G OSBORNE STEVEN J OSBORNE
2	<u>STEPHEN PHILIP OSBORNE</u> <a href="#">Get More Info</a>	54	HAYWARD, CA ✓ CANYON COUNTRY, CA ✓ WOODLAND HILLS, CA ✓ MIDDLETON, WI ✓ SANTA MONICA, CA ✓	✓	✓	✓	CYNTHIA CROSBY OSBORNE
3	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	34	OCALA, FL	✓	✓	✓	STEVEN P OSBORNE
4	<u>STEPHEN PAUL OSBORNE</u> <a href="#">Get More Info</a>	49	GARLAND, TX FORNEY, TX	✓	✓	✓	THERESA OSBORNE AMIE OSBORNE BLAKE OSBORNE WUT T OSBORNE ALETA JOYCE OSBORNE JOYCE CHANEY OSBORNE JERRY WILLIAM OSBORNE
5	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	34	OCALA, FL	✓	✓	✓	STEVEN P OSBORNE JAIME OSBORNE
6	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	49	MILAN, TN MEDINA, TN	✓	✓	✓	
7	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	51	CHULA VISTA, CA BONITA, CA SAN DIEGO, CA	✓	✓	✓	BERIT OSBORNE MAXINE L OSBORNE DIANE APRIL OSBORNE LINDA N OSBORNE
8	<u>STEPHEN PATRICK OSBORNE</u> <a href="#">Get More Info</a>	43	DELAND, FL	✓	✓	✓	STEVE LEE OSBORNE SARA L OSBORNE
9	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	85	PITTSBURGH, PA	-	✓	✓	MARY J OSBORNE STEVE OSBORNE
10	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	40	BOCA RATON, FL NEWARK VALLEY, NY SAINT PETERSBURG, FL TAMPA, FL OLDSMAR, FL PINELLAS PARK, FL	✓	✓	✓	STEVEN P OSBORNE
	NAME	AGE	PREVIOUS CITIES	DOB	PHONE	ADDRESS	RELATIVES

STEPHEN PATRICK OSBORNE

11	<a href="#">Get More Info</a>	58	NEWHALL, CA	✓	✓	✓	RYAN OSBORNE Delfina Osbourne Cary F Osbourne
12	<a href="#">Get More Info</a>	58	VALENCIA, CA	✓	✓	✓	D OSBORNE STEVE OSBORNE
13	<a href="#">Get More Info</a>	34	OCALA, FL	✓	✓	✓	
14	<a href="#">Get More Info</a>	51	DELAND, FL	✓	✓	✓	SARA L OSBORNE
15	<a href="#">Get More Info</a>	49	MESQUITE, TX	✓	✓	✓	THERESA M OSBORNE
16	<a href="#">Get More Info</a>	-	BUTTE, MT	-	✓	✓	
17	<a href="#">Get More Info</a>	-	BUTTE, MT	-	✓	✓	JOHN OSBORNE BETTY OSBORNE JANET L OSBORNE SHARON MAE OSBORNE STEVE P OSBORNE ELIZABETH OSBORNE WILLIAM JOHN OSBORNE
18	<a href="#">Get More Info</a>	23	RODMAN, NY	✓	✓	✓	CAROLYN H OSBORNE DANIEL CAROLYN OSBORNE
19	<a href="#">Get More Info</a>	34	OCALA, FL	✓	-	✓	STEVEN P OSBORNE
20	<a href="#">Get More Info</a>	34	OCALA, FL	✓	-	✓	STEVEN P OSBORNE

NAME	AGE	PREVIOUS CITIES	DOB	PHONE	ADDRESS	RELATIVES
STEPHEN P OSBORNE	34	OCALA, FL	✓	✓	✓	IRENE C OSBORNE NELLIE J OSBORNE YVONNE O OSBORNE
STEPHEN P OSBORNE	85	PITTSBURGH, PA	-	-	✓	MARY J OSBORNE JAMES W OSBORNE
STEPHEN P OSBORNE	36	LYNN, MA	✓	-	✓	STEVE P OSBORNE
STEPHEN P OSBORNE	58	PHOENIX, AZ	✓	-	✓	JOHN S OSBORNE
STEPHEN P OSBORNE	34	OCALA, FL	✓	-	✓	

26	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	59	CANYON COUNTRY, CA ✓	-	-	✓	
27	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	55	HOUSTON, TX	✓	-	✓	
28	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	NORMAN, OK	-	✓	✓	
29	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	46	DENVER, CO	-	-	✓	
30	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	51	SAN DIEGO, CA	✓	-	✓	
	NAME	AGE	PREVIOUS CITIES	DOB	PHONE	ADDRESS	RELATIVES
31	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	ENDICOTT, NY	-	✓	✓	
32	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	55	SANTA CLARA, CA ✓	✓	-	✓	
33	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	CHULA VISTA, CA	-	-	✓	
34	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	BUTTE, MT	-	-	✓	
35	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	BUTTE, MT	-	-	✓	
36	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	YUMA, AZ	-	✓	✓	STEVE P OSBORNE
37	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	51	CHULA VISTA, CA	✓	-	✓	
38	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	PINELLAS PARK, FL	-	-	✓	
39	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	-	PACOIMA, CA	-	-	✓	
40	<u>STEPHEN P OSBORNE</u> <a href="#">Get More Info</a>	31	IRWIN, PA	✓	-	✓	
	NAME	AGE	PREVIOUS CITIES	DOB	PHONE	ADDRESS	RELATIVES

STEPHEN P OSBORNE

41

SANTA MONICA, CA

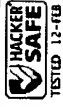


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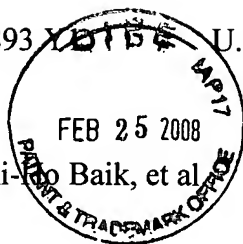
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§ EXAMINER: B.L. Raymond

§

§

§ ATTORNEY DOCKET NO.:

§

AM-8893 Y1

**EXHIBIT "C"**

**LETTER SENT TO INVENTOR OSBORNE**

PLEASE PRESS FIRMLY

PLEASE PRESS FIRMLY



Flat Rate  
Mailing Envelope

UNITED STATES POSTAL SERVICE

For Domestic and International Use

Visit us at [usps.com](http://usps.com)



EB 796042834 US



internationally  
is declarations  
76, or 2976A).



Mailing Label  
Label 11-B, March 2004

Post Office To Addressee

UNITED STATES POSTAL SERVICE®

DELIVERY ATTEMPT		Time	Employee Signature
Mo.	Day	<input type="checkbox"/> AM <input type="checkbox"/> PM	
Mo.	Day	<input type="checkbox"/> AM <input type="checkbox"/> PM	
Mo.	Day	<input type="checkbox"/> AM <input type="checkbox"/> PM	
Mo.	Day	<input type="checkbox"/> AM <input type="checkbox"/> PM	

**CUSTOMER USE ONLY**

**WAVES OF SIGNATURE (Domestic Mail Only)**  
Additional merchandise insurance is void if customer requests waiver of signature.  
I wish delivery to be made without obtaining signature. I understand that the carrier will deliver the mail (if delivery employee judges that article can be left in secure location) and I authorize that delivery employee's signature constitutes valid proof of delivery.

Express Mail Corporate Acct. No. \_\_\_\_\_  
Federal Agency Acct. No. or Postal Service Acct. No. \_\_\_\_\_

☐ NO DELIVERY ☐ Holiday ☐ Mailer Signature \_\_\_\_\_

TO: (PLEASE PRINT) PHONE ( 858 ) 587-6633

Shirley L. Church, Esq.  
P.O. Box 81146  
San Diego, CA

ZIP + 4 (U.S. ADDRESSES ONLY. DO NOT USE FOR FOREIGN POSTAL CODES.)

9	2	1	3	8	+	1	1	4	6
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**ORIGIN (POSTAL SERVICE USE ONLY)**

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Stephen Osborne  
1228 D Street  
Hayward, CA 94541  
AM-8893 Y1

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---

January 18, 2008

**Via Express Mail**

Mr. Stephen Osborne  
1228 D Street  
Hayward, CA 94541

RE: U.S. Patent Application No.: 10/817,140  
For: "Method of Improving the Uniformity of a Patterned Resist on Photomask"  
Filed: April 2, 2004  
Our Ref. No.: AM-8893 Y1

Dear Mr. Osborne:

We are filing a Request for Continued Examination of the above-referenced application of which you are an inventor. We are enclosing a copy of a *Declaration of Prior Invention Under 37 CFR § 1.131* for your signature. We need your signature to proceed with the application.

Also enclosed are a copy of the patent application as filed and a copy of the invention alert showing critical dates for your reference. A self-addressed envelope is included for the return of the signed Declaration of Prior Invention

As you may know, inventors must **sign and date** the Declaration to be accepted by the PTO. Also, all hand-written changes must be initialed by the inventor making such changes. Please return the signed and dated Declaration to us by **February 1, 2008** so that we may file the document with the U.S. Patent Office in a timely manner.

We thank you so much for your assistance in this matter. Please do not hesitate to contact us if you have any questions or comments.

With my best regards,

By:   
Shirley L. Church, Esq.

SLC:lsg  
Enclosures

cc: Maureen Walstra, Patent Administrator (via email only)  
[patent\\_office@amat.com](mailto:patent_office@amat.com) (via email only)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

§ GROUP ART UNIT: 1756

SERIAL NO.: 10/817,140

§

§

FILED: April 2, 2004

§

§ EXAMINER: B.L. Raymond

§

§

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK

§

§ Attorney Docket No.:

§ AM-8893

Date: \_\_\_\_\_, 2008

**DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131****Mail Stop AF****Hon. Commissioner for Patents****P.O. Box 1450****Alexandria, VA 22313-1450**

Sir:

This Declaration under 37 CFR § 1.131 accompanies Response "B", which is in response to the Office Action mailed July 25, 2007.

We, Ki-Ho Baik, Mark A. Mueller, Stephen Osborne, Robert Dean, and Homer Lem hereby declare that we are joint inventors of the invention claimed in U.S. Patent Application Serial No. 10/817,140. We further declare that said invention was conceived and reduced to practice by us prior to January 6, 2004, which is the filing date of U.S. Patent Application Serial No. 10/752,885, which was published on December 30, 2004, as U.S. Publication No. 2004/0266113.

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**CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

I hereby certify that this paper and any documents said to accompany this paper are being deposited with the U.S. Postal Service on the date shown below with sufficient postage as U.S. EXPRESS MAIL NO. EB 450583747 US in an envelope addressed to : Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: \_\_\_\_\_, 2008

\_\_\_\_\_  
Shirley L. Church, Reg. No.31,858

In support of our Declaration, attached is a copy of the Invention Alert which preceded the present patent application. This Invention Alert was prepared by us and sent electronically to the docketing department of Applied Materials, Inc. on 11/21/2003. Subsequently, the Invention Alert was returned to us for signature, and signatures were obtained between December 17 and December 18, 2003. The signatures were witnessed on December 18, 2003, a Docket No. of 8893 was assigned, and the Invention Alert was scheduled to be sent out to an attorney for preparation of a patent application on that date.

Portions of the Invention Alert which pertain to conclusory dates of invention have been dedacted to protect the rights of the inventors.

We, the undersigned, each declare that all statements made herein are of his own knowledge true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements and the like may jeopardize the validity of the application or any patent issued thereon.

1)	_____	_____
		Ki-Ho Baik, Co-inventor
2)	_____	_____
		Mark A. Mueller, Co-inventor
3)	_____, 2008	_____
		Stephen Osborne, Co-inventor
4)	_____	_____
		Robert Dean, Co-inventor
5)	_____	_____
		Homer Lem, Co-inventor

**ALERT NO:**

# INVENTION ALERT FORM

Date: 11/21/2003

**TO: Gaile Bailey M/S 2061/Extension 32724**

**CIRCLE ONLY ONE FROM TOP ROW (REQUIRED FIELD):-**

# MASK/ETEC

[illegible]

1. Title of Invention (please print clearly): **Vacuum Treatment for Improvement of Uniformity of Patterned Resist on a Photomask and Wafer**
2. Inventors: Names only. (please print clearly and provide complete information at Section 9.)

**Ki-Ho Baik, Mark Mueller, Steve Osborne, Robert Dean, Homer Lem**

Please use separate attachments for any answers that don't fit on the form, especially for questions 3-8. If the answer to a question is "NONE", please write "NONE" rather than leaving the answer blank.

3. Earliest dates and model names of all Applied products incorporating the invention which have been offered for sale or are expected to be offered for sale:

Mebes eXara, electron beam photomask writer,

RSB, electron beam photomask writer,

Tetra1, photomask etcher,

Tetra2, photomask etcher,

4. If the invention has been demonstrated or described to persons other than Applied employees, for each disclosure please provide the earliest date, name of company, a brief description of what was disclosed and the purpose of the disclosure. Attach a copy of any related non-disclosure agreements:

NOT described outside Applied Materials, not yet disclosed.

5. If future disclosures like those in Question #4 are expected to occur within the next 12 months, please provide the anticipated date, type of information to be disclosed, and purpose of the disclosure:

NONE [ ]

This invention would be most useful for ETEC to meet its technical specifications and commitments at IBM, where an RSB is being evaluated and compared to a competing product. Therefore it would be in Applied Materials' business interests to disclose this invention to IBM as soon as possible, in order to improve the ETEC-RSB product performance and gain a competitive advantage.

Preliminary data shows an improvement in resist local CD uniformity as a result of vacuum treatment. CD uniformity improvement in resist is between zero and 1 nm 3sigma, which is significant.

This invention is expected to be of significant interest to the photomask user community. Thus publication, after patent filing protection of IP, would serve Applied Materials' interests in advertising lithographic patterning capabilities.

6. Describe any other known designs or processes, whether actually implemented or merely proposed in a publication, which could be considered similar to your invention or which constitute the state-of-the-art improved upon by your invention: If described in a publication, attach a copy of same or provide a citation.

No known publications describe anything similar to this invention.

A broad search on the US Patent Office website (USPTO.com) scanning for the phrase "resist AND vacuum AND (semiconductor OR lithography OR photomask)" in claims turned up no previous patent which has any similarity to the invention proposed here. There are no reported applications of vacuum processing which claim or report what we are listing below as a novel and non-obvious feature.

The state-of-the-art electron beam photomask processing sequence is summarized:

1. Photomask is coated with resist, post-<sup>application</sup> exposure baked (PAB), and exposed (electron beam or

laser used for creating a pattern onto the photomask resist).

2. The photomask is post-exposure baked (PEB) and developed, which removes the unpatterned resist from the plate.
3. The photomask is then etched, whereby the resist pattern is transferred into an underlying chrome layer. Additional etching may be required for phase-shift masks (PSM).



7. List each feature of the invention which you consider novel and non-obvious. Describe the advantages of each novel feature in comparison with the state-of-the-art approaches which are most similar to your invention:

**Novel and Non-Obvious Features:**

- 1) Use of a post-develop, pre-etch vacuum processing step to reduce variation in critical dimensions on photomasks. The advantage of such a processing step is of enormous benefit to photomask manufacturers. By reducing variation in critical dimensions, the quality of the photomask is improved.

State of the art: No specific vacuum treatment of photomask. The photomask is simply developed, air exposed (and possibly measured in a CD-SEM to get resist CD information), and then the chrome is etched.

- 2) Use of vacuum to alter the composition and dimensions of resist features on a photomask. By applying a vacuum to a photomask (or wafer) for about 20 minutes, water vapor and solvent are desorbed by the surface of the resist. This may enable surface tension (or other mechanisms not yet studied in complete detail) to minimize roughness on the sidewall of a resist feature, which reduces line edge roughness (LER) and also reduces CD variation. Vacuum processing affects the mean CD by only a few nanometers.

State of the art: One commonly applied means of altering resist dimensions on a photomask (or wafer) is the use of a "descum" oxygen plasma step. This basically burns away a fixed amount of resist, which unfortunately reduces the resist dimensions by at least 30nm, but also may also help to smoothen line edges. Descum treatment is not applicable to small feature lithography, since this step consumes a significant amount of lateral resist.

- 3) Application of vacuum treatment to reduce Line Edge Roughness (LER) on resist lines on a photomask (patterned by either electron beam or laser).

State of the art: Descum (see #3 above).

- 4) Application of vacuum to a photomask plate in a photomask etching chamber in which chamber walls and dome are heated, allowing the resist on the photomask to warm to a temperature between 30 degrees C and 55 degrees C, which enables the desorption from the surface of the resist of water vapor, solvents, and materials absorbed onto the surface from the develop process step and other previous steps. In particular, the Applied Materials Tetra etching system is used for this vacuum treatment. Photomasks are placed into a chamber for 20 minutes of vacuum time, where the 55 degree chamber wall and 70 degree dome radiate heat onto the photomask plate. Longer times do not provide any improvement in desorption. The "curve" of resist change is observed to flatten out at 20 minutes.

- 5) Application of a vacuum treatment to a photomask (or wafer) after electron beam exposure (or laser or other methods of resist exposure) to reduce critical dimension variation.

Preliminary data from delayed removal of a photomask from the RSB electron beam writer has shown that CD uniformity may be slightly improved. A nine-hour delay time was utilized in this preliminary work. Delayed removal places the photomask in vacuum for a longer period, prior to air exposure and immediate Post-Exposure Bake. It is possible to perform this vacuum treatment in a Tetra (Applied Materials photomask etcher) chamber, where the vacuum treatment does not impact the RSB throughput. It is also possible to perform the vacuum treatment in other vacuum chambers.

- 6) Generalization of #1 through 5 to include wafers and other substrates. General application to wafers can improve the quality of lithography in the patterning of wafers. Specifically, this can be applied to all wafer lithographic processes where critical dimension control is required, for all wavelengths of light utilized in wafer lithography (G-line, i-line, KrF, ArF, 157) plus other methods used for patterning resist on wafers, such as e-beam, FIB, X-ray, and EUV. Line edge roughness is reduced, and critical dimension control is improved.

8. Describe the invention, preferably with reference to attached drawings:

The invention consists of an additional processing step in the standard "state of the art" sequence described above in Part 6. This is specifically a vacuum applied to the photomask between Step 2 and Step 3 (as noted above in Part 6). Proper timing of the vacuum allows for desorption of materials from the resist surface. Such desorption is found to slightly decrease the thickness of the resist layer. In addition, a slight shrinkage of pattern dimension is observed in the lateral (photomask plane) directions. Moreover, our data shows an improvement in Local CD Uniformity, in which crosses of a given fixed size are printed within a 1mm square, and then measured. Variations in local CD Uniformity can be attributed to a) various electron beam fluctuations during resist patterning and b) process-related line-edge roughness. The ETEC process has succeeded in drastically reducing the latter by creating a proprietary resist and fine-tuning all of the resist-related processing parameters. However, we believe at this time that vacuum processing is capable of further reduction in line-edge roughness, resulting in reduced Local CD Uniformity.

★ Two types of vacuum treatment are described above in the previous section. Vacuum treatment can be applied to a photomask immediately after exposure and before PEB (Post Exposure Bake). This enables acids within the resist to diffuse in such a way as to improve contrast and to reduce line edge roughness.

Another vacuum treatment is applied to the photo-mask after develop. In this second vacuum treatment, water vapor and solvents are desorbed from the surface of the patterned resist. In this case, the surface includes sidewalls and the top resist surface. By desorbing the volatile components, the resist loses material and that part of resist close to the surface is in tension. This surface tension may allow for the "pulling together" of the surface which may smooth out sidewall roughness. Since the tension does not apply to the bulk of the resist (deeper than within a few nanometers of the surface), lines and other features are not distorted.

ATTACH ADDITIONAL SHEETS TO DESCRIBE INVENTION AS NEEDED

Provide the following information for EACH inventor\*\* REQUIRED FIELDS:

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 Product Group: ETEC Dept #: 0667

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 Product Group: ETEC Cost Center #: 0667

**Inventor #3:**

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<b>Inventor #4:</b>			
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Job Title:	<u>Member of Technical Staff</u>		
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Home Address:	<u>5306 Greenridge Rd., Castro Valley, CA 94582</u>		
Manager	<u>Ki-Ho Baik</u>	Title:	<u>Sr. Director</u>
Div. Manager	<u>Ronen Ben Tzion</u>	Title:	<u>General Manager</u>
Product Group:	<u>ETEC</u>	Dept #:	<u>0667</u>

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Legal Name: \_\_\_\_\_ Employee # \_\_\_\_\_ Mail Stop \_\_\_\_\_  
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Div. Manager \_\_\_\_\_ Title: \_\_\_\_\_  
Product Group: \_\_\_\_\_ Dept #: \_\_\_\_\_

10. Signature, date and PRINTED name of each inventor plus two witnesses who have read and understood this Invention Alert form:

**Inventors:**MARK MUELLER

Printed Name

12/17/03

Date

Mark Mueller

Signature

Robert Dean

Printed Name

12/17/03

Date

[Signature]

Signature

K. Ho BATIC

Printed Name

12/17/03

Date

[Signature]

Signature

HOMER LEM

Printed Name

12/18/03

Date

Homer Lem

Signature

STEVEN OSBURN

Printed Name

12/18/03

Date

St. Osburn

Signature

Printed Name

Date

Signature

**Witness:**DAMON M. COLE

Printed Name

12/18/03

Date

Damon M. Cole

Signature

Allen R. Cook

Printed Name

12/18/03

Date

Allen R. Cook

Signature

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1 [0001] **METHOD OF IMPROVING THE UNIFORMITY OF A PATTERNED**  
2 **RESIST ON A PHOTOMASK**

3 [0002] 1. Field of the Invention

4 [0003] In general, the present invention relates to a method of producing a photomask  
5 (reticle) for use in the semiconductor industry. In particular, the invention pertains to a  
6 method for improving the critical dimension (CD) uniformity of a pattern in a photoresist  
7 which is used to transfer the pattern to a reticle.

8 [0004] 2. Brief Description of the Background Art

9 [0005] Photoresists are used in microlithographic processes to produce patterned features  
10 required for device functioning in miniaturized electronic components, such as in the  
11 fabrication of semiconductor device structures. The miniaturized electronic device structure  
12 patterns are typically created using blanket radiation through a photomask to produce a  
13 pattern in a layer of photoresist material present on a semiconductor structure. There are  
14 instances, for specialized devices, where a pattern is directly written into a photoresist  
15 present on the semiconductor structure; however, due to the slow production speed of the  
16 direct write process, this is not commonly done.

17 [0006] A photomask or reticle which is used to enable rapid semiconductor device  
18 processing typically includes a thin layer of a radiation-blocking material (which is often a  
19 metal-containing material, such as a chrome-containing, molybdenum-containing, or  
20 tungsten-containing layer, for example) deposited on a glass or quartz plate. The thin layer  
21 of radiation-blocking material is patterned to contain a "hard copy" of the pattern to be  
22 recreated on the photoresist or photoresist / hard mask layer overlying a semiconductor  
23 structure. The patterning of the radiation-blocking layer of a reticle may be carried out using  
24 a number of different techniques. Due to the dimensional requirements of today's  
25 semiconductor structures, the pattern is typically generated using a direct write laser or  
26 e-beam to create a latent image in a photoresist for subsequent transfer to the radiation-



1 blocking layer.

2 [0007] The reticle manufacturing process generally includes the following steps, when  
3 the initial substrate used to form the reticle is a silicon oxide-containing base layer having  
4 a layer of a metal-containing (typically chrome) mask material applied thereover. An  
5 inorganic antireflective coating (ARC) or an organic ARC, or a combination of inorganic  
6 and organic ARC layers, may be applied over the surface of the chrome mask material. A  
7 photoresist layer is then applied over the antireflective coating. The photoresist is typically  
8 an organic material which is dissolved in a solvent. The solution of photoresist is typically  
9 spin coated onto the surface of the photomask fabrication structure. Some of the solvent is  
10 removed during the spin coating operation. Residual solvent is subsequently removed by  
11 another means, typically by baking the fabrication structure, including the photoresist layer.  
12 This step is commonly referred to as a "post-apply bake" or PAB. The photoresist is then  
13 exposed to radiation (imaged), to produce a pattern in the photoresist layer, typically by a  
14 direct write process when the pattern includes dimensions which are less than about  $0.4\ \mu\text{m}$   
15 or less. After exposure, the substrate including the photoresist layer is baked again. The  
16 second baking is typically referred to as a "post-exposure bake" or PEB. The photoresist  
17 is then developed, either using a dry process or a wet process, to create the pattern having  
18 openings through the photoresist layer thickness. Once the photoresist is "patterned" so that  
19 the pattern openings extend through the photoresist layer to the upper surface of an ARC  
20 layer, or to a surface beneath an ARC layer, the pattern in the patterned photoresist is  
21 transferred through the chrome-based mask layer and any remaining layers overlying the  
22 chrome layer, for example, typically by dry etching.

23 [0008] As described above, preparation of a photomask / reticle is a complicated process  
24 involving a number of interrelated steps which affect the critical dimensions of a pattern  
25 produced in the reticle and the uniformity of the pattern critical dimensions across the  
26 surface area of the reticle. Various efforts have been made within the industry to improve  
27 the reliability of manufacturing processes by improving individual process steps; however,  
28 when a production process involves a number of interrelated process steps, alteration of an

1 individual process step may have an unexpected result on other interrelated process steps.

2 [0009] Commonly owned U.S. Patent No. 6,703,169, to Scott Fuller et al., issued March  
3 9, 2004, and entitled "Method of Preparing Optically Imaged High Performance  
4 Photomasks", discloses a state-of-the-art method of fabricating a photomask using optical  
5 radiation in the form of a direct write continuous wave laser. The claimed method  
6 comprises a series of steps including: applying an organic antireflection coating over a  
7 metal-containing layer; applying a chemically-amplified positive tone or negative tone DUV  
8 photoresist over the organic antireflection coating, to provide a photoresist-coated  
9 photomask substrate; post-apply baking the DUV photoresist over a temperature ranging  
10 from about 105°C to about 115°C; exposing a surface of the DUV photoresist to radiation  
11 from the direct write continuous wave laser, to provide a patterned photoresist across the  
12 photomask substrate; and post-exposure baking the DUV photoresist over a temperature  
13 ranging from about 70°C to about 90°C. The post-apply bake process provides increased  
14 stability period for the photoresist-coated photomask substrate, where there is less than a  
15 5 nm change in a 400 nm latent image critical dimension after a 6-hour time period. A  
16 combination of the post-apply bake process and the post-exposure bake process results in  
17 a uniform critical dimension of the patterned photoresist across the photomask substrate,  
18 where, for a 132-mm x 132-mm active area, a critical dimension uniformity is  $\leq 10$  nm at  
19 400 nm. The disclosure of U.S. Patent No. 6,703,169 is hereby incorporated by reference  
20 in its entirety.

21 [0010] Commonly owned, co-pending U.S. Application Serial No. 10/768,919, of  
22 Christopher Dennis Bencher et al., filed January 30, 2004, and entitled "Reticle Fabrication  
23 Using a Removable Hard Mask", discloses a method of fabricating a reticle which provides  
24 improved critical dimension uniformity during fabrication of a reticle by minimizing the  
25 problem known as "photoresist pull-back", which commonly occurs during etching of a  
26 chrome (or other radiation-blocking layer) on a reticle substrate. According to the method  
27 disclosed by Bencher et al., pattern transfer to the radiation-blocking layer of the reticle  
28 substrate essentially depends upon transfer from a hard mask rather than from a photoresist.

1 In one embodiment, a hard mask material having anti-reflective properties is left on the  
2 surface of the chrome after etching of the chrome. Since the hard mask surface faces the  
3 surface of a photoresist on the semiconductor substrate which is patterned using the reticle,  
4 the presence of the proper anti-reflective properties in the hard mask can be used to reduce  
5 the amount of bounce-back of reflected radiation which occurs during blanket radiation  
6 imaging of the semiconductor photoresist through the reticle. In another embodiment, where  
7 a wet etch is used during fabrication of the reticle, the hard mask material (whether having  
8 anti-reflective properties or not) is removed to prevent contamination during the wet etch  
9 process. In this embodiment, when a plasma etchant used to remove the hard mask would  
10 also etch the reticle base substrate (which is typically quartz), a protective layer is applied  
11 to fill at least a portion of patterned openings through the chrome during removal of the hard  
12 mask. This prevents etching of the quartz at the bottom of the pattern openings during  
13 removal of the hard mask. The disclosure of U.S. Application Serial No. 10/768,919 is  
14 hereby incorporated by reference in its entirety.

15 [0011] As device dimensions become even smaller, further improvements in critical  
16 dimension uniformity of photomasks are needed. One commonly used means of improving  
17 photomask dimensional uniformity is by improving the dimensions of the patterned  
18 photoresist used to transfer the pattern to the photomask. The patterned photomask may be  
19 "descummed" using an oxygen plasma step, in which surface defects are removed from the  
20 photoresist pattern. Exposure to the oxygen plasma basically burns away a fixed amount  
21 of resist, which may help to smooth pattern line edges. Unfortunately, however, the descum  
22 oxygen plasma step typically reduces the resist dimensions by about 20 - 30 nm, making the  
23 descum process inapplicable to very small feature lithography.

24 [0012] It is readily apparent that it would be highly desirable to have a method of making  
25 a photomask where the uniformity of pattern critical dimensions is maintained across the  
26 entire surface of the photomask, even for features smaller than about 100 nm. To provide  
27 an improved photomask, it would be very advantageous to provide an improved patterned  
28 photoresist which can be used to transfer the pattern directly to the photomask, or to transfer

1 the pattern to a hard mask which is subsequently used to pattern the photomask.

2 [0013] **SUMMARY OF THE INVENTION**

3 [0014] We have discovered that application of a vacuum to a pattern irradiated (imaged)  
4 photoresist prior to development of the photoresist provides an improvement in critical  
5 dimension and uniformity in the developed photoresist. This improvement is translated into  
6 an improvement in the patterned photomask produced using the photoresist.

7 [0015] Typically, the application of vacuum is carried out prior to a post-exposure bake  
8 of the kind which is commonly performed on an imaged photoresist prior to development.  
9 Exposure of the photoresist on the photomask substrate to vacuum is performed for a period  
10 of time sufficient to allow the imaged pattern critical dimensions to reach equilibrium across  
11 the photoresist. The vacuum treatment process allows reaction by-product, water vapor, and  
12 solvents, for example, to desorb from the surface of the resist, improving critical dimension  
13 uniformity across the surface of the photoresist on the photomask substrate.

14 [0016] Typically, exposure of the pattern-imaged photoresist to vacuum is performed at  
15 a substrate temperature within the range of about 18°C to about 60°C (more typically,  
16 within the range of about 18°C to about 40°C), for a period of time within the range of  
17 about 10 minutes to about 70 hours (more typically, within the range of about 20 minutes  
18 to about 12 hours), at a process chamber pressure ranging from about  $5 \times 10^{-6}$  mTorr to  
19 about 5 mTorr. The pressure within the processing chamber during the vacuum treatment  
20 process may be limited by the capability of the particular apparatus in which the vacuum  
21 treatment process is performed. For example, when the vacuum treatment process is  
22 performed in an Applied Materials' \_\_\_\_\_ e-beam direct-write apparatus  
23 following the pattern writing process, the process chamber pressure during the vacuum  
24 treatment process is typically about  $1 \times 10^{-5}$  mTorr. When the vacuum treatment process is  
25 performed in an Applied Materials' TETRA™ etch system, the process chamber pressure  
26 during the vacuum treatment process may vary between about \_\_\_\_\_ mTorr to about \_\_\_\_\_  
27 mTorr, and was typically in the range of about 0.5 mTorr to about 1 mTorr during the

1 experimentation described herein.

2 [0017] The time period required for pattern critical dimensions to reach equilibrium  
3 across the photoresist will depend upon the photoresist layer composition, and a  
4 combination of the temperature of the substrate / photoresist during the vacuum treatment  
5 process and the pressure (vacuum) applied. The minimal time period required for vacuum  
6 treatment of the photoresist on the photomask substrate will be the time period which  
7 provides no substantial change in pattern critical dimensions upon continued exposure of the  
8 irradiated photoresist to the vacuum.

9 [0018] Typically, the higher the temperature, the less time is required for pattern critical  
10 dimensions to reach equilibrium. However, the temperature is limited by the general  
11 stability of the photoresist material, which will depend on the particular photoresist material  
12 used. Also, typically the lower the pressure in the process chamber, the less time is required  
13 for vacuum treatment at a given temperature; however, the pressure used must ensure that  
14 deformation of the pattern does not occur and that the integrity of the photoresist is  
15 preserved. The amount of time required will also depend upon the condition of the  
16 photoresist prior to the vacuum treatment process, which will depend upon the type of  
17 photoresist used, the solvents in the photoresist, and the length of time of the post-apply  
18 bake (PAB) process. With minimal experimentation, one skilled in the art will be able to  
19 integrate the vacuum treatment step into an existing process for photomask production.

20 [0019] We have also discovered that exposure of the patterned (developed) photoresist  
21 to vacuum after development results in an improvement in the line edge roughness of pattern  
22 openings that have been formed through the photoresist layer thickness. This second  
23 vacuum treatment process is typically performed at a substrate temperature within the range  
24 of about 20°C to about 60°C for a period of time within the range of about 10 minutes to  
25 about 60 minutes, at a process chamber pressure ranging from about  $5 \times 10^{-6}$  mTorr to about  
26 5 mTorr, where the time period is a function of the combination of temperature and pressure.  
27 In this second vacuum treatment, water vapor and solvents absorbed during the development  
28 process are desorbed from surfaces of the patterned resist, including the sidewalls and top

1 resist surface. During desorption of the volatile components, the portion of the resist which  
2 is close to the surface is placed in tension. It is theorized, but not intended as a limitation,  
3 that this surface tension may allow for the “pulling together” of the surface, which may  
4 smooth out sidewall roughness. Since the bulk of the resist (deeper than within a few  
5 nanometers of the surface) is not in tension, lines and other features are not distorted.

6 [0020] The vacuum treatment processes of the invention work well whether the  
7 photoresist on the photomask substrate has been exposed to electron beam (e-beam) or  
8 optical radiation. Vacuum processing of photomask substrates according to the method of  
9 the invention typically improves the mean CD of the patterned photoresist by reducing the  
10 variation from the intended CD by about 3 nm or more, and by improving the uniformity  
11 (3-sigma) across a substrate surface by about 3 - 5 nm.

12 [0021] **BRIEF DESCRIPTION OF THE DRAWINGS**

13 [0022] Figure 1A shows a schematic cross-sectional view of a typical embodiment of a  
14 beginning structure 100 of a stack of materials used in the production of a photomask or  
15 reticle, when the pattern is transferred from the photoresist to the radiation-blocking layer  
16 of the mask without the use of a hard mask. The stack from bottom to top includes a  
17 substrate 102, which is typically selected from quartz, fluorinated quartz, borosilicate glass,  
18 or soda lime glass; a radiation-blocking layer 104, which is typically a metal-containing  
19 layer selected from a chromium, molybdenum silicide, or tungsten-containing layer, or  
20 combinations thereof (in the examples described herein, the radiation-blocking layer is  
21 essentially chrome); an inorganic ARC layer 105; an organic ARC layer 106; and a  
22 photoresist layer 108.

23 [0023] Figure 1B shows the Figure 1A structure 100 after development of the photoresist  
24 layer 108 to create a pattern of lines and spaces in the photoresist layer 108.

1 [0024] Figure 2 is a graph 200 showing a global cross 1 x CD uniformity (in nm)  
2 following vacuum treatment of the imaged photoresist prior to development, when the  
3 substrates were vacuum treated in a MEBES™ QUADRA™ imaging system ("RSB  
4 Vacuum") or were vacuum treated in an Applied Materials' TETRA™ etch chamber ("Tetra  
5 Vacuum"), compared with the global CD uniformity for substrates which received no  
6 vacuum treatment following exposure of the photoresist to radiation ("No Vacuum").

7 [0025] Figure 3 is a graph 300 showing the decrease in developed photoresist thickness  
8 302 as a function of time under vacuum 304, for photomask substrates which were vacuum  
9 treated in accordance with the present invention. The substrates were vacuum treated in an  
10 Applied Materials' TETRA™ etch chamber, at a temperature of approximately 45°C and  
11 a process chamber pressure of approximately 0.5 mTorr.

12 [0026] Figure 4 is a graph 400 showing local CD uniformity (in nm) before and after  
13 vacuum treatment of the developed photoresist. The substrates were vacuum treated in an  
14 Applied Materials' TETRA™ etch chamber for a period of 20 minutes, at a temperature of  
15 approximately 30°C and a process chamber pressure of approximately 1 mTorr.

16 [0027] **DETAILED DESCRIPTION OF THE INVENTION**

17 [0028] We have discovered a method of improving the patterning of a layer of  
18 photoresist which has been applied over a photomask substrate. The present method results  
19 in improved critical dimension uniformity of the developed photoresist. In general, the  
20 method comprises the steps of: a) post-apply baking the photoresist; b) exposing the  
21 photoresist to imaging radiation (typically direct-write radiation); c) exposing the imaged  
22 photoresist to a vacuum for a period of time sufficient to allow pattern critical dimensions  
23 to equilibrate across the photoresist, at a process chamber pressure ranging from about  
24  $5 \times 10^{-6}$  mTorr to about 5 mTorr (typically, at a temperature ranging from about 20°C to  
25 about 60°C, and for a time period ranging from about 10 minutes to about 70 hours);

1 d) post-exposure baking the imaged photoresist; and e) developing the imaged photoresist  
2 to create a pattern having openings through the photoresist layer thickness.

3 [0029] The method may further comprise the additional step f) of exposing the developed  
4 photoresist to a vacuum subsequent to step e), at a substrate temperature within the range  
5 of about 20°C to about 60°C for a period of time within the range of about 10 minutes to  
6 about 60 minutes, at a process chamber pressure ranging from about  $5 \times 10^{-6}$  mTorr to about  
7 5 mTorr. This second vacuum exposure step has been shown to improve the line edge  
8 roughness of pattern openings that have been formed through the photoresist layer thickness.

9 [0030] As a preface to the detailed description presented below, it should be noted that,  
10 as used in this specification and the appended claims, the singular forms “a”, “an”, and “the”  
11 include plural referents, unless the context clearly dictates otherwise.

12 [0031] I. METHOD OF PATTERNING A PHOTORESIST ON A PHOTOMASK  
13 SUBSTRATE

14 [0032] All methods of patterning a photomask substrate may benefit from application of  
15 the present method. The method is particularly useful for DUV optical or e-beam patterning  
16 of a photomask when a chemically amplified photoresist is used to transfer the pattern to the  
17 photomask. The present Examples are for a REAP™ 200 chemically amplified photoresist  
18 (available from Tokyo Ohka Kogyo Co., Ltd. (TOK), Kawasaki, Japan), which is useful  
19 with both e-beam radiation and 248 nm optical radiation. However, the scope of the  
20 invention is not intended to be limited to this family of chemically amplified photoresists.

21 [0033] Figure 1A shows one embodiment of a starting structure 100 used in the  
22 fabrication of example photomasks for experimental purposes herein. In this Example,  
23 starting structure 100 was a stack of layers (not shown to scale) which included, from top  
24 to bottom, a 3000 Å thick layer 108 of a chemically amplified photoresist, REAP™ 200  
25 (available from TOK, Kawasaki, Japan); a 500 Å thick layer 106 of an organic ARC  
26 identified as XLT-BARC (available from Brewer Science, Inc., Rolla, MO); a 300 Å thick  
27 layer 105 of chromium oxynitride inorganic ARC; a 400 Å thick layer 104 of chrome mask



1 material; and a silicon oxide-containing substrate 102.

2 [0034] The starting structure 100 shown in Figure 1A can be formed using conventional  
3 deposition techniques known in the art of semiconductor manufacture. In particular, the  
4 photoresist layer 108 is typically applied to the surface of the organic ARC layer 106 using  
5 spin-on coating techniques. Some of the solvent or dispersion medium is removed during  
6 the spin coating operation.

7 [0035] Photoresist compositions of the kind suitable for use in the present method  
8 include: REAP™ 200 and EN24 (both available from TOK, Kawasaki, Japan); NEB 22  
9 (available from Sumitomo Chemical Co., Ltd., Tokyo, Japan); and FEP 171 and FEN 270  
10 (both available from Fuji-Hunt Electronics Company, Tokyo, Japan), by way of example  
11 and not by way of limitation.

12 [0036] After application of the photoresist layer, applicants performed a post-apply bake  
13 (PAB) process to remove residual solvent or dispersion medium. The post-apply bake  
14 process is typically performed at a temperature within the range of about 70°C to about  
15 150°C, for a time period of about 4 minutes to about 30 minutes. A particularly useful post-  
16 apply bake process is described in detail in U.S. Patent No. 6,703,169, to Fuller et al., the  
17 disclosure of which is incorporated by reference in its entirety.

18 [0037] After post-apply bake, the photoresist was exposed to radiation (imaged), to  
19 produce a latent pattern in the photoresist layer, typically by a direct write process when the  
20 pattern includes dimensions which are less than about 0.4  $\mu\text{m}$ . In the example embodiment,  
21 the minimum pattern dimension was about 60 nm. In the exposure process, the integrated  
22 circuit patterns were direct written onto the unpatterned photoresist 108 coated on a mask  
23 blank which included organic ARC layer 106, inorganic ARC layer 105, chrome-containing  
24 layer 104, and quartz layer 102 (described above). In a different embodiment, a hard mask  
25 (not shown) may be present between the photoresist 108 and the radiation-blocking layer  
26 104.

27 [0038] The vacuum treatment process of the invention works well whether imaging of  
28 the photoresist is by e-beam radiation or by optical radiation. In the examples described

1        herein, imaging of the photoresist was performed in a MEBES™ QUADRA™ electron  
2        beam mask patterning system (available from ETEC Systems, Inc., an Applied Materials  
3        company, with Applied Materials, Inc., having offices in Santa Clara, CA). Other imaging  
4        systems which can be used to practice the method described herein include, without  
5        limitation, the MEBES™ eXara™ electron beam mask patterning system, and the ALTA™  
6        3900 and ALTA™ 4300 laser beam mask patterning systems (all available from ETEC  
7        Systems, Inc.).

8        [0039]    After imaging of the photoresist on the photomask substrate, the imaged  
9        photoresist was treated with a vacuum for a period of time sufficient to allow pattern critical  
10       dimensions to reach equilibrium across a given photoresist layer. The time period required  
11       for latent, imaged pattern critical dimensions to reach equilibrium across the photoresist will  
12       depend upon a combination of the temperature of the substrate during the vacuum treatment  
13       process and the pressure (vacuum) applied. After exposure of the imaged photoresist on the  
14       photomask substrate to vacuum for an optimum time period, no substantial change in pattern  
15       critical dimensions will occur upon continued exposure of the imaged photoresist to  
16       vacuum.

17       [0040]    Typically, the higher the temperature, the less time is required for imaged pattern  
18       critical dimensions to reach equilibrium. However, the temperature is limited by the general  
19       stability of the photoresist material, which will depend on the particular photoresist material  
20       used. Also, typically the lower the pressure in the process chamber, the less time is required  
21       at a given temperature; however, the pressure used must ensure that deformation of the  
22       pattern does not occur and that the integrity of the photoresist is preserved. The amount of  
23       time required will also depend upon the condition of the photoresist prior to the vacuum  
24       treatment process, which will depend upon the type of photoresist used, the solvents in the  
25       photoresist, and the length of time of the post-apply bake (PAB) process. With minimal  
26       experimentation, one skilled in the art will be able to determine the amount of time required  
27       based on the particular apparatus that s/he is using and the particular process conditions  
28       under which that apparatus typically operates.

1 [0041] Vacuum treatment of photomask substrates in accordance with the methods of the  
2 invention can be performed in any suitable semiconductor processing apparatus which is  
3 capable of maintaining a process chamber pressure within the range of about  $5 \times 10^{-6}$  mTorr  
4 to about 5 mTorr. For example, an imaged photomask substrate may be vacuum treated in  
5 the exposure tool used for direct-write pattern irradiation of the photoresist. Alternatively,  
6 vacuum treatment of the imaged photomask substrates can be performed in other available  
7 equipment, for example, and not by way of limitation, in an Applied Materials' TETRA™  
8 photomask etch system. By moving the photomask substrates to a different chamber for  
9 vacuum treatment following imaging, exposure tool throughput is not affected.

10 [0042] Typically, exposure of the imaged photoresist on the photomask substrate to  
11 vacuum is performed at a substrate temperature within the range of about 18°C to about  
12 60°C (more typically, within the range of about 18°C to about 40°C. Heating of the imaged  
13 resist on the photomask substrate to a temperature within the range of about 30°C to about  
14 60°C, and at a pressure ranging from about 0.1 mTorr to about 5 mTorr provides a  
15 substantial improvement in imaged resist pattern uniformity after a treatment.

16 [0043] Figure 2 is a graph 200 showing global cross 1 x CD uniformity 202 (in nm)  
17 following vacuum treatment of the imaged photoresist prior to development, where the  
18 substrates were vacuum treated in the MEBEST™ QUADRA™ imaging system ("RSB  
19 Vacuum") 204 or were vacuum treated in an Applied Materials' TETRA™ etch chamber  
20 ("Tetra Vacuum") 206, compared with the global CD uniformity for substrates which  
21 received no vacuum treatment following exposure of the photoresist to radiation ("No  
22 Vacuum") 208. The RSB Vacuum substrates were vacuum treated in the pattern writing  
23 apparatus for a period of 5 - 9 hours at approximately 21 - 22°C), at a process chamber  
24 pressure of approximately  $1 \times 10^{-5}$  mTorr. The Tetra Vacuum substrates were vacuum  
25 treated in a TETRA™ etcher for a period of 30 minutes at a temperature of approximately  
26 30°C, at a process chamber pressure of approximately 1 mTorr. The substrates which  
27 received no vacuum treatment were maintained at approximately 21 - 22°C.

1 [0044] After vacuum treatment, the photoresist was baked again. The second baking step  
2 is typically referred to as a "post-exposure bake" or PEB. Chemical reaction takes place  
3 between the time the pattern is written by irradiation upon the photoresist and the PEB, but  
4 after the PEB, the latent image is essentially fixed within the photoresist. The amount of  
5 time and the temperature of the substrate (*i.e.*, the time / temperature profile) depends on the  
6 photoresist, and one skilled in the art can determine what this should be in view of the  
7 photoresist manufacturer's recommendations.

8 [0045] The post-exposure bake process is typically performed at a temperature within the  
9 range of about 70°C to about 150°C, for a time period of about 4 minutes to about  
10 30 minutes. A particularly useful post-exposure bake process is described in detail in U.S.  
11 Patent No. 6,703,169, to Scott Fuller et al., the disclosure of which is incorporated by  
12 reference in its entirety.

13 [0046] After post-exposure bake, the photoresist is developed, either using a dry process  
14 or a wet process, to create the pattern having openings through the photoresist layer  
15 thickness. The photoresist in the present instance was developed using a puddle or spray  
16 develop process with a TMAH (2.38 weight % or 1.91 weight %) developer.

17 [0047] We have also discovered that exposure of the patterned (developed) photoresist  
18 to vacuum after development results in an improvement in the line edge roughness of pattern  
19 openings that have been formed through the photoresist layer thickness. Accordingly, after  
20 development of the photoresist, the method of the invention may further comprise an  
21 optional step of exposing the photoresist to a vacuum at a substrate temperature within the  
22 range of about 20°C to about 60°C for a period of time within the range of about 10 minutes  
23 to about 60 minutes, at a process chamber pressure ranging from about  $5 \times 10^{-6}$  mTorr to  
24 about 5 mTorr.

25 [0048] In this second vacuum treatment, water vapor and solvents absorbed during the  
26 development process are desorbed from surfaces of the patterned resist, including the  
27 sidewalls and top resist surface. During desorption of the volatile components, the portion  
28 of the resist which is close to the surface is placed in tension. It is theorized, but not

1 intended as a limitation, that this surface tension may allow for the “pulling together” of the  
2 surface, which may smooth out sidewall roughness. Since the bulk of the resist (deeper than  
3 within a few nanometers of the surface) is not in tension, lines and other features are not  
4 distorted.

5 [0049] Proper timing of the vacuum treatment process allows for desorption of water  
6 vapor, solvents, and other by-products of previous processing steps from the surface of the  
7 resist, and also enables acids within the resist to diffuse in such a way as to reduce line edge  
8 roughness. Desorption of materials from the resist was found to slightly decrease the  
9 thickness of the photoresist layer. In addition, a slight shrinkage of pattern dimension was  
10 observed in the lateral (photomask plane) directions. Overall, vacuum processing of  
11 photomask substrates according to the method of the invention typically improves the mean  
12 CD of the patterned photoresist by reducing the variation of the intended CD by  
13 approximately 3 nm or more, and by improving the uniformity (3 sigma) across the wafer  
14 by about 3 - 5 nm. Our data also show an improvement in local CD uniformity.

15 [0050] Figure 3 is a graph 300 showing the decrease in photoresist thickness 302 for a  
16 developed photoresist as a function of time under vacuum 304 for photomask substrates  
17 which were vacuum treated in accordance with the present invention. The “curve” 306 of  
18 resist change is observed to “flatten out” (*i.e.*, reach equilibrium) after about 20 minutes of  
19 vacuum treatment, after which no substantial change in pattern critical dimensions was  
20 observed upon continued exposure of the imaged photoresist to vacuum. The substrates  
21 were vacuum treated in an Applied Materials’ TETRA™ etch chamber for a period of 20  
22 minutes, at a temperature of approximately 45°C, and a process chamber pressure of  
23 approximately 0.5 mTorr.

24 [0051] The data presented graphically in Figure 3 is for the REAP™ 200 photoresist.  
25 Data were also obtained for the EN24 photoresist (available from TOK, Kawasaki, Japan)  
26 and FEP 171 photoresist (available from Fuji-Hunt Electronics Company, Tokyo, Japan),  
27 under the same processing conditions described above for the REAP™ 200 photoresist.  
28 These data are presented in Table One, below.

[0052] Table One. Decrease in Photoresist Thickness Following Post-Exposure Vacuum Treatment

Photoresist	Decrease in Photoresist Thickness (Å)
REAP™ 200	20
EN24	23
FEP 171	17

[0053] Figure 4 is a graph 400 showing local CD uniformity 402 (in nm) before ("PreVac CDU") and after ("PostVac CDU") vacuum treatment of the developed photoresist. The substrates were vacuum treated in an Applied Materials' TETRA™ etch chamber for 20 minutes, at a temperature of approximately 30°C and a process chamber pressure of approximately 1 mTorr. Local CD variations for the y direction pre-vacuum treatment 404 and post-vacuum treatment 406 are shown for a first sample ("Sample # 1"). Local CD variations for the y direction pre-vacuum treatment 408 and post-vacuum treatment 410, are also shown for a second sample ("Sample # 2"). The two photomask substrate samples had different line-and-space patterns, which would explain the variation in CD uniformity between the two samples. The data shown in Figure 4 are for a REAP™ photoresist (available from TOK, Kawasaki, Japan).

[0054] In addition to their use in the preparation of photomasks, the vacuum treatment processes described herein can be used to improve the quality of lithography in the patterning of semiconductor wafers. The vacuum treatment processes described herein can be applied to all wafer lithographic processes where critical dimension control is required, for all wavelengths of light utilized in wafer optical and e-beam lithography (G-line, i-line, KrF, ArF, 257 nm, for example, and not by way of limitation), plus other methods used for patterning resist on wafers, such as EUV. Line edge roughness is reduced, and critical dimension control is improved.

1 [0055] Figure 1B shows a schematic cross-sectional view of the patterned photoresist  
2 layer 108 (prior to transfer of the pattern through underlying organic ARC layer 106,  
3 inorganic ARC layer 105, and chrome-containing layer 104), where the pattern was lines  
4 107 and spaces 111, where the line width was about 30 nm to about 3  $\mu\text{m}$  and the spacing  
5 between lines was about 30 nm to about 3  $\mu\text{m}$ .

6 [0056] Once the photoresist has been developed and "patterned", so that the pattern  
7 openings extend through the photoresist layer to the upper surface of an ARC layer, or to a  
8 surface beneath an ARC layer, subsequent processing steps are typically performed in order  
9 to transfer the pattern in the patterned photoresist through the chrome-based mask layer and  
10 any remaining layers overlying the chrome layer. These subsequent processing steps are  
11 summarized below and are also described in detail in U.S. Patent No. 6,703,169, to Scott  
12 Fuller et al., which is incorporated by reference herein in its entirety. The mask fabrication  
13 process transforms the latent image created by the exposure of the photoresist into a  
14 permanent chrome image on the quartz substrate.

15 [0057] The pattern in the photoresist is typically transferred to the underlying photomask  
16 structure using a dry etch process, such as a plasma etching process. The chrome oxynitride  
17 (inorganic ARC) / chrome mask layer etch is typically performed using a plasma generated  
18 from a chlorine / oxygen / helium gas mixture. Typically, higher oxygen concentrations and  
19 lower pressures cause higher mean-to-target deviation and lower selectivities, while favoring  
20 better CD uniformity control. Plasma etch systems such as the TETRA™ etch system  
21 (available from Applied Materials, Inc., of Santa Clara, CA) may be used to provide  
22 excellent results. However, one skilled in the art will be able to optimize the process for  
23 other plasma etch apparatus.

24 [0058] Typically, the chrome layer is overetched beyond endpoint to clear residual  
25 chrome from all open regions. Generally, the overetch step is an extension of the chrome  
26 etch process described above. Longer overetch steps result in higher mean-to-target  
27 deviations. Chrome spot defect densities can be affected by the length of overetch, with  
28 lower defect densities for longer overetch processes.

1 [0059] After completion of the chrome layer etch, a strip and clean process is typically  
2 performed to remove any residual contaminants from the surface of the chrome layer. The  
3 strip process may be performed by heating sulfur peroxide to about 75°C and applying the  
4 heated sulfur peroxide over the surface of the substrate plate. After treatment with sulfuric  
5 peroxide, the substrate plate is typically rinsed with CO<sub>2</sub>-reionized or CO<sub>2</sub>-sparged deionized  
6 water. After strip, the substrate plate is typically subjected to an acid clean using an industry  
7 standard 70 : 30 H<sub>2</sub>SO<sub>4</sub> / H<sub>2</sub>O<sub>2</sub> solution, followed by another deionized water rinse. For  
8 example, the strip step may be performed on a Steag ASC 500 wet chemical processing  
9 station, available from STEAG-HAMMATECH® (Santa Clara, CA).

10 [0060] The above described preferred embodiments are not intended to limit the scope  
11 of the present invention, as one skilled in the art can, in view of the present disclosure,  
12 expand such embodiments to correspond with the subject matter of the invention claimed  
13 below.



[0061]

**CLAIMS**

We claim:

1        1.        In a method of patterning a layer of photoresist which has been applied over a  
2        photomask substrate and exposed to imaging radiation, the improvement comprising  
3        exposing said imaged photoresist to a vacuum for a period of time sufficient to allow pattern  
4        critical dimensions to equilibrate across said photoresist, at a process chamber pressure  
5        ranging from about  $5 \times 10^{-6}$  mTorr to about 5 mTorr.

1        2.        A method in accordance with Claim 1, wherein exposure of said imaged  
2        photoresist to said vacuum is performed at a substrate temperature within the range of about  
3        18°C to about 60°C, for a period of time within the range of about 10 minutes to about  
4        70 hours.

1        3.        A method in accordance with Claim 2, wherein exposure of said imaged  
2        photoresist to said vacuum is performed at a substrate temperature within the range of about  
3        18°C to about 40°C, for a period of time within the range of about 20 minutes to about  
4        12 hours.

1        4.        A method in accordance with Claim 1, wherein said radiation is e-beam radiation.

1        5.        A method in accordance with Claim 1, wherein said radiation is optical radiation.

1        6.        A method in accordance with Claim 1, wherein exposure of said imaged  
2        photoresist to said vacuum is performed prior to the performance of a post-exposure bake  
3        process.

1        7.        A method in accordance with Claim 1, wherein said exposure of said imaged  
2 photoresist to said vacuum is performed prior to development of said photoresist to create  
3 a pattern having openings through said photoresist layer thickness.

1        8.        In a method of patterning a layer of photoresist which has been applied over a  
2 photomask substrate, exposed to imaging radiation, and developed to create a pattern having  
3 openings through said photoresist layer thickness, the improvement comprising exposing  
4 said developed photoresist to a vacuum at a substrate temperature within the range of about  
5 20°C to about 60°C for a period of time within the range of about 10 minutes to about  
6 60 minutes, at a process chamber pressure ranging from about  $5 \times 10^{-6}$  mTorr to about 5  
7 mTorr.

1        9.        A method of patterning a layer of photoresist which has been applied over a  
2 photomask substrate, comprising:

- 3            a)        post-apply baking said photoresist;  
4            b)        exposing said photoresist to imaging radiation;  
5            c)        exposing said imaged photoresist to a vacuum for a period of time  
6 sufficient to allow pattern critical dimensions to equilibrate across said photoresist, at a  
7 process chamber pressure ranging from about  $5 \times 10^{-6}$  mTorr to about 5 mTorr;  
8            d)        post-exposure baking said imaged photoresist; and  
9            e)        developing said imaged photoresist to create a pattern having openings  
10 through said photoresist layer thickness.

1        10.        A method in accordance with Claim 9, wherein exposure of said imaged  
2 photoresist to said vacuum is performed at a substrate temperature within the range of about  
3 18°C to about 60°C, for a period of time within the range of about 10 minutes to about  
4 70 hours.

1 11. A method in accordance with Claim 10, wherein exposure of said imaged  
2 photoresist to said vacuum is performed at a substrate temperature within the range of about  
3 18°C to about 40°C, for a period of time within the range of about 20 minutes to about  
4 12 hours.

1 12. A method in accordance with Claim 9, wherein said radiation is e-beam radiation.

1 13. A method in accordance with Claim 9, wherein said radiation is optical radiation.

1 14. A method in accordance with Claim 9, wherein said method further includes the  
2 following step:

3 f) exposing said developed photoresist to a vacuum at a substrate  
4 temperature within the range of about 20°C to about 60°C for a period of time within the  
5 range of about 10 minutes to about 60 minutes, at a process chamber pressure ranging from  
6 about  $5 \times 10^{-6}$  mTorr to about 5 mTorr.

1 15. A method of patterning a layer of photoresist which has been applied over a  
2 photomask substrate, comprising:

3 a) post-apply baking said photoresist;  
4 b) exposing said photoresist to imaging radiation;  
5 c) post-exposure baking said imaged photoresist;  
6 d) developing said imaged photoresist to create a pattern having openings  
7 through said photoresist layer thickness; and  
8 e) exposing said developed photoresist to a vacuum at a substrate  
9 temperature within the range of about 20°C to about 60°C for a period of time within the  
10 range of about 10 minutes to about 60 minutes, at a process chamber pressure ranging from  
11 about  $5 \times 10^{-6}$  mTorr to about 5 mTorr.

1        16.        A method in accordance with Claim 15, wherein said imaging radiation is e-beam  
2        radiation.

1        17.        A method in accordance with Claim 15, wherein said imaging radiation is optical  
2        radiation.

1 [0062]

**ABSTRACT OF THE DISCLOSURE**

2 [0063] We have discovered that exposure of a photoresist on a photomask substrate to  
3 a vacuum after the photoresist has been exposed to imaging radiation results in improved  
4 critical dimension uniformity of the developed photoresist. Exposure of the imaged  
5 photoresist to vacuum is performed for a period of time sufficient to allow pattern critical  
6 dimensions to reach equilibrium across the photoresist. The vacuum treatment process of  
7 the invention is typically performed prior to the performance of a post-exposure bake  
8 process and prior to development of the photoresist. We have also discovered that exposure  
9 of a photoresist on a photomask substrate to a vacuum after the photoresist has been  
10 developed results in an improvement in the line edge roughness of pattern openings that  
11 have been formed through the photoresist layer thickness.

Fig. 1A  
(Prior Art)

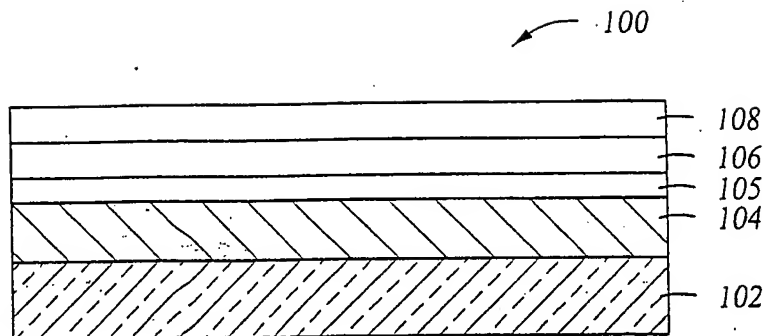
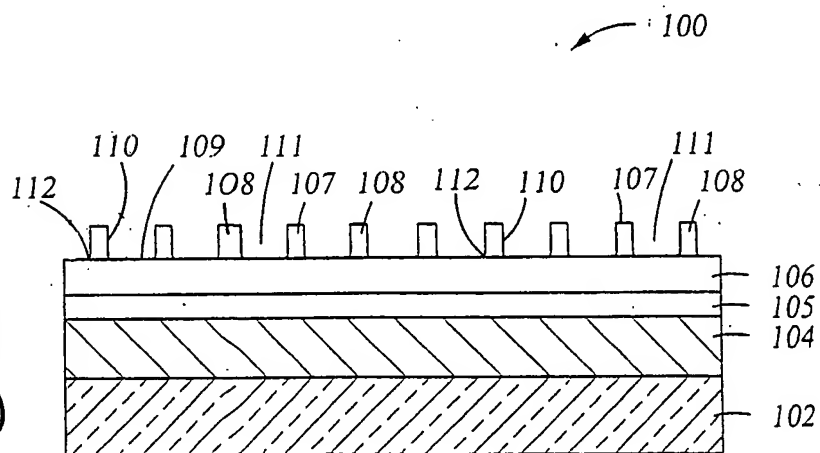


Fig. 1B  
(Prior Art)



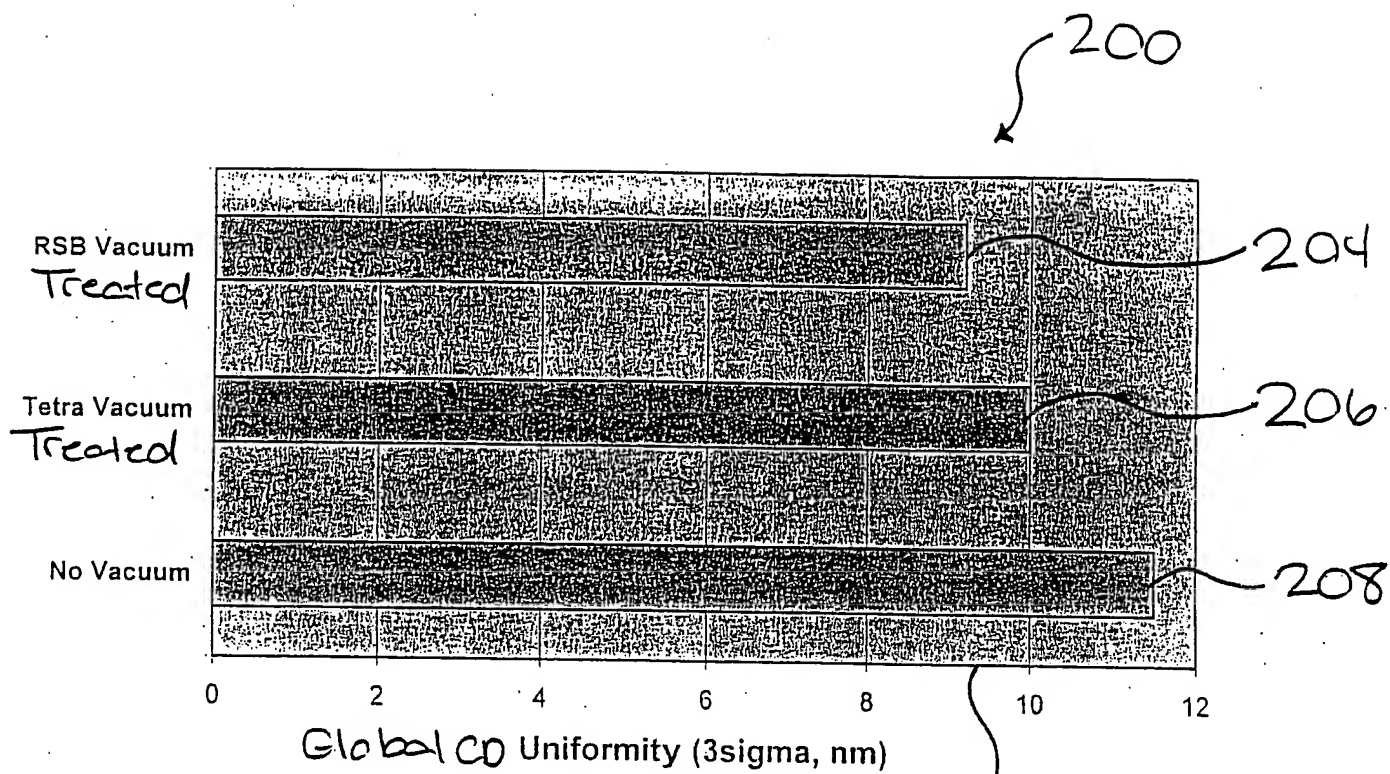


FIG. 2

202

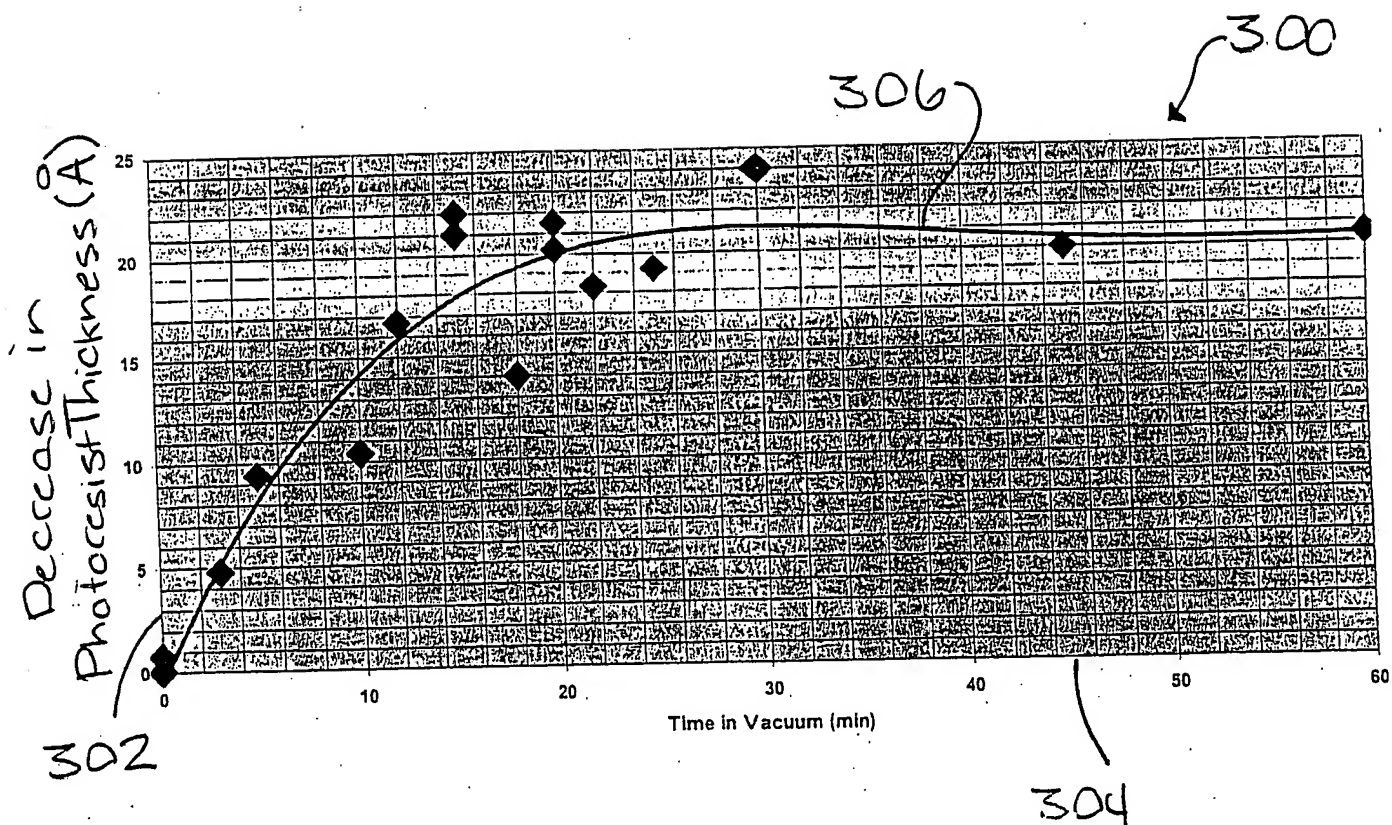


FIG. 3



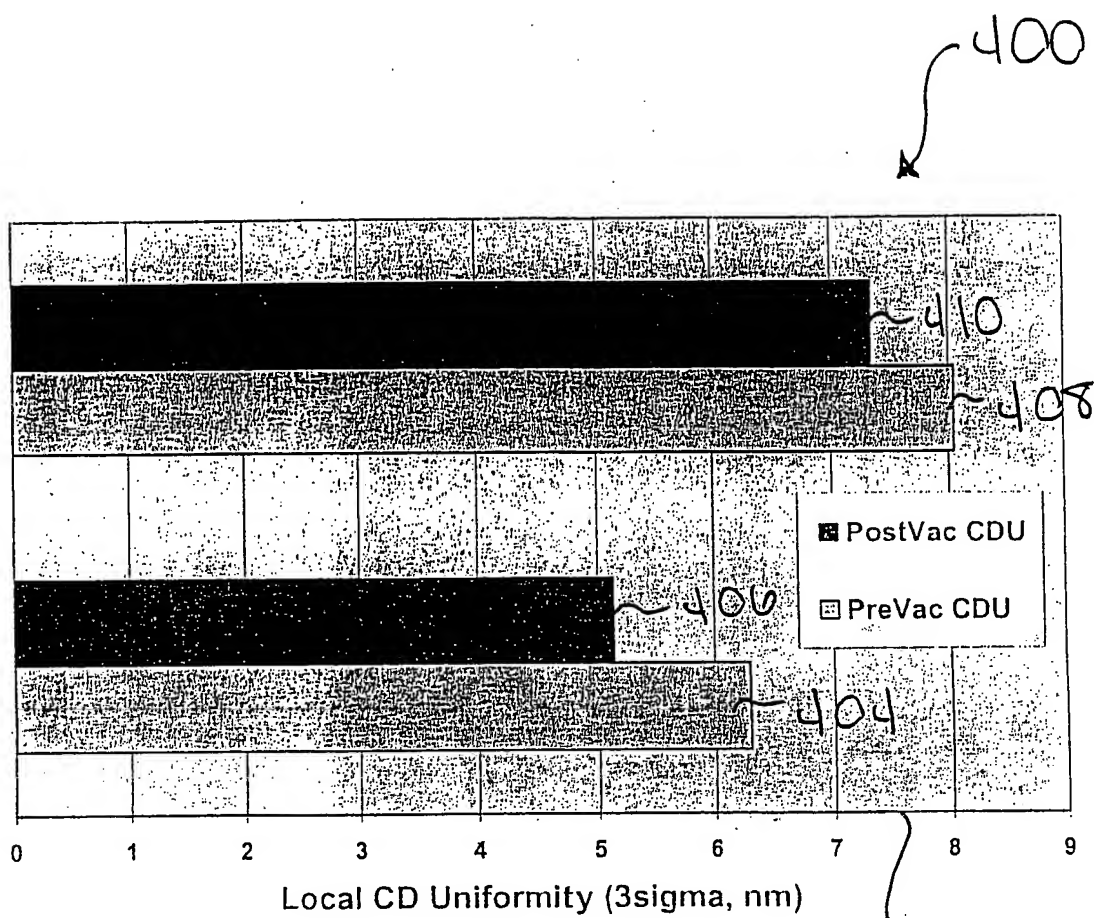


Fig. 4

IN RE APPLICATION OF: Ki-Ho Baik, et al.

SERIAL NO.: 10/817,140

FILED: April 2, 2004

FOR: METHOD OF IMPROVING THE  
UNIFORMITY OF A PATTERNED RESIST ON A  
PHOTOMASK

§ GROUP ART UNIT: 1763

§

§

§ EXAMINER: B.L. Raymond

§

§

§ ATTORNEY DOCKET NO.:  
§ AM-8893 Y1

**EXHIBIT "D"**

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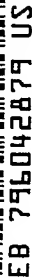
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Date Accepted <u>1-19-08</u> M'd <u>19</u> Day <u>08</u> Year <u>08</u>		Flat Rate <input type="checkbox"/> or Weight <u>9.73</u> lbs.		Int'l Alpha Country Code <u>...</u> Acceptance Fee <u>...</u>	

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

§ GROUP ART UNIT: 1756

SERIAL NO.: 10/817,140

§

§

FILED: April 2, 2004

§

§ EXAMINER: B.L. Raymond

§

§

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK

§ Attorney Docket No.:  
AM-8893

Date: February 25, 2008

**DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131**

**Mail Stop Petition**

**Hon. Commissioner for Patents**

**P.O. Box 1450**

**Alexandria, VA 22313-1450**

Sir:

This Declaration is to be combined with the Declaration Under 37 CFR § 1.131 which was filed in response accompanies Response "B", which is in response to the Office Action mailed July 25, 2007.

Ki-Ho Baik, Mark A. Mueller, Stephen Osborne, Robert Dean, and Homer Lem are joint inventors of the invention claimed in U.S. Patent Application Serial No. 10/817,140. I, Homer Lem, declare that said invention was conceived and reduced to practice by the above-named inventors prior to January 6, 2004, which is the filing date of U.S. Patent Application Serial No. 10/752,885, which was published on December 30, 2004, as U.S. Publication No. 2004/0266113.

---

**CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

I hereby certify that this paper and any documents said to accompany this paper are being deposited with the U.S. Postal Service on the date shown below with sufficient postage as U.S. EXPRESS MAIL NO. EB 450583747 US in an envelope addressed to : Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: February 25, 2008

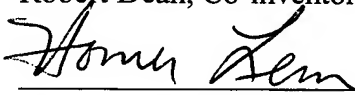
  
Shirley L. Church, Reg. No. 31,858

---

In support of our Declaration, attached is a copy of the Invention Alert which preceded the present patent application. This Invention Alert was prepared by us and sent electronically to the docketing department of Applied Materials, Inc. on 11/21/2003. Subsequently, the Invention Alert was returned to us for signature, and signatures were obtained between December 17 and December 18, 2003. The signatures were witnessed on December 18, 2003, a Docket No. of 8893 was assigned, and the Invention Alert was scheduled to be sent out to an attorney for preparation of a patent application on that date.

Portions of the Invention Alert which pertain to conclusory dates of invention have been dedacted to protect the rights of the inventors.

We, the undersigned, each declare that all statements made herein are of his own knowledge true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements and the like may jeopardize the validity of the application or any patent issued thereon.

1)	_____	_____	Ki-Ho Baik, Co-inventor
2)	_____	_____	Mark A. Mueller, Co-inventor
3)	_____	_____	Stephen Osborne, Co-inventor
4)	_____	_____	Robert Dean, Co-inventor
5)	<u>Jan. 22</u> , 2008		Homer Lem, Co-inventor

**COPY**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

SERIAL NO.: 10/817,140

RCE FILED: October 25, 2007

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK



§ GROUP ART UNIT: 1756

§ (In parent case)

§

§ EXAMINER: B.L. Raymond

§ (In parent case)

§

§

§ Attorney Docket No.:

§ AM-8893 Y1

Date: October 25, 2007

**PETITION IN SUPPORT OF**  
**DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131**

Director Technology Center 1700  
or Primary Examiner Group Art Unit 1756  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

1. This Petition accompanies a Request for Continued Examination Under 37 C.F.R. § 1.114.  
The Request for Continued Examination is being made to permit applicants to place the  
application in better condition for appeal.

**CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

I hereby certify that this paper and any documents said to accompany this paper are being deposited with  
the U.S. Postal Service on the date shown below with sufficient postage as U.S. EXPRESS MAIL NO.  
EB 450583835 US in an envelope addressed to : Mail Stop RCE, Commissioner for Patents, P.O. Box  
1450, Alexandria, VA 22313-1450.

Date: October 25, 2007

*Shirley L. Church*  
Shirley L. Church, Reg. No. 31,858

2. This Petition is in support of the Declaration under 37 CFR § 1.131 which accompanied Response "B", which was made in reply to the Office Action mailed July 25, 2007. Examiner Raymond (Examiner of the parent application to the present RCE) informed applicants' attorney, in a telephone conversation, that the Declaration was not acceptable, because it was not signed by all of the inventors, and because no Petition requesting acceptance of the Declaration without the presence of signatures by all of the inventors accompanied the Declaration.

3. Applicants' attorney explained to the Examiner that the Declaration was supported by a copy of the "Invention Alert" submitted by the inventors to their employer. The Invention Alert was signed by all of the inventors, and showed a date prior to the critical date with respect to the reference at issue. Further, applicants' attorney mentioned that the Response "B" which accompanied the Declaration explained that the ETEC Division of Applied Materials, Inc. which had employed the inventors had been disbanded, and that none of the inventors were currently employed by Applied Materials, Inc. Employer, Applied Materials, Inc., furnished past known addresses for the previous employees, but only three of these employees could be located by applicants' attorney. The signatures of the three inventors are present on the Declaration Under 37 CFR § 1.131 which was previously submitted, and which is presently being re-submitted with this Petition.

4. The parent application to the present RCE application is under final rejection. Applicants' attorney recognized that it was unlikely that a Petition would be considered in time to permit a timely appeal. Further, applicants had very good arguments as to why the reference which was the subject of the Declaration Under 37 CFR § 1.131 was distinguishable art from the present invention. Applicants' attorney was hopeful that after a telephone interview with the Examiner, the application could be allowed without the need to file an RCE which would provide time for consideration of a Petition.



5. On October 23, 2007, the Examiner contacted applicants' attorney to inform her that after final consideration, the Examiner was not willing to allow the application. Applicants' attorney is of the opinion that it will be necessary to appeal the rejection of the application to the Board of Patent Appeals & Interferences. Applicants would therefore like to have the reference which is the subject of the Declaration Under 37 CFR § 1.131 removed from consideration, and are submitting this petition so that the Declaration will be accepted despite the absence of the signatures of a portion of the inventors. As was discussed above, the Declaration is supported by an evidentiary document signed by all of the inventors which shows a date of invention prior to the critical date.

6. In view of the above, the Director Technology Center 1700 or a Primary Examiner of Group Art Unit 1756 is respectfully requested to grant the present Petition and to permit the acceptance of applicants' Declaration Under 37 CFR § 1.131.

7. This Petition is accompanied by the fee required under 37 CFR § 1.17(f).

Respectfully submitted,



Shirley L. Church  
Registration No. 31,858  
Attorney for Applicants  
(858) 587-6633

Correspondence Address:  
Customer No. 60767  
Shirley L. Church, Esq.  
P.O. Box 81146  
San Diego, California 92138

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

§ GROUP ART UNIT: 1756

SERIAL NO.: 10/817,140

§

§

§ EXAMINER: B.L. Raymond

FILED: April 2, 2004

§

§

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK

§

§ Attorney Docket No.:

§ AM-8893

Date: October 9, 2007**DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131**

Mail Stop AF

Hon. Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

This Declaration under 37 CFR § 1.131 accompanies Response "B", which is in response to the Office Action mailed July 25, 2007.

We, Ki-Ho Baik, Mark A. Mueller, Stephen Osborne, Robert Dean, and Homer Lem hereby declare that we are joint inventors of the invention claimed in U.S. Patent Application Serial No. 10/817,140. We further declare that said invention was conceived and reduced to practice by us prior to January 6, 2004, which is the filing date of U.S. Patent Application Serial No. 10/752,885, which was published on December 30, 2004, as U.S. Publication No. 2004/0266113.

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Date: October 9, 2007

  
Shirley L. Church, Reg. No. 31,858

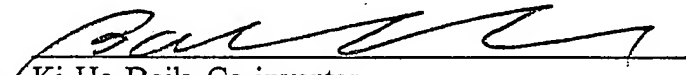
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We, the undersigned, each declare that all statements made herein are of his own knowledge true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements and the like may jeopardize the validity of the application or any patent issued thereon.

1) October 4, 2007

  
Ki-Ho Baik, Co-inventor

2) October \_\_\_\_\_, 2007

\_\_\_\_\_  
Mark A. Mueller, Co-inventor

3) October \_\_\_\_\_, 2007

\_\_\_\_\_  
Stephen Osborne, Co-inventor

4) October \_\_\_\_\_, 2007

\_\_\_\_\_  
Robert Dean, Co-inventor

5) October \_\_\_\_\_, 2007

\_\_\_\_\_  
Homer Lem, Co-inventor

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

§ GROUP ART UNIT: 1756

SERIAL NO.: 10/817,140

§

§

FILED: April 2, 2004

§

§ EXAMINER: B.L. Raymond

§

§

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK

§

§ Attorney Docket No.:

§ AM-8893

Date: October 9, 2007**DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131**

Mail Stop AF  
Hon. Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

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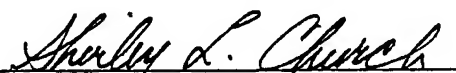
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Date: October 9, 2007

  
Shirley L. Church, Reg. No. 31,858

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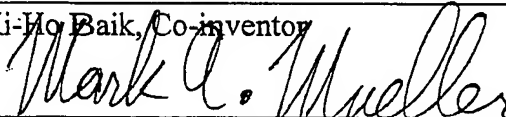
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1) October \_\_\_\_, 2007

Ki-Ho Baik, Co-inventor

2) October 3, 2007

  
Mark A. Mueller, Co-inventor

3) October \_\_\_\_, 2007

Stephen Osborne, Co-inventor

4) October \_\_\_\_, 2007

Robert Dean, Co-inventor

5) October \_\_\_\_, 2007

Homer Lem, Co-inventor

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Ki-Ho Baik et al.

§ GROUP ART UNIT: 1756

SERIAL NO.: 10/817,140

§

§

§ EXAMINER: B.L. Raymond

FILED: April 2, 2004

§

§

FOR: METHOD OF IMPROVING THE UNIFORMITY OF  
A PATTERNED RESIST ON A PHOTOMASK

§

§ Attorney Docket No.:

§ AM-8893

Date: October 9, 2007**DECLARATION OF PRIOR INVENTION UNDER 37 CFR § 1.131****Mail Stop AF****Hon. Commissioner for Patents****P.O. Box 1450****Alexandria, VA 22313-1450**

Sir:


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Date: October 9, 2007

  
Shirley L. Church, Reg. No. 31,858

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1) October \_\_\_\_, 2007

\_\_\_\_\_  
Ki-Ho Baik, Co-inventor

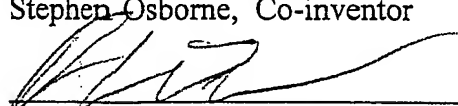
2) October \_\_\_\_, 2007

\_\_\_\_\_  
Mark A. Mueller, Co-inventor

3) October \_\_\_\_, 2007

\_\_\_\_\_  
Stephen Osborne, Co-inventor

4) October 4, 2007

  
\_\_\_\_\_  
Robert Dean, Co-inventor

5) October \_\_\_\_, 2007

\_\_\_\_\_  
Homer Lem, Co-inventor





Please use separate attachments for any answers that don't fit on the form, especially for questions 3-8. If the answer to a question is "NONE", please write "NONE" rather than leaving the answer blank.

3. Earliest dates and model names of all Applied products incorporating the invention which have been offered for sale or are expected to be offered for sale:

Mebes eXara, electron beam photomask writer,

RSB, electron beam photomask writer,

Tetra1, photomask etcher,

Tetra2, photomask etcher,

4. If the invention has been demonstrated or described to persons other than Applied employees, for each disclosure please provide the earliest date, name of company, a brief description of what was disclosed and the purpose of the disclosure. Attach a copy of any related non-disclosure agreements:

NOT described outside Applied Materials, not yet disclosed.

5. If future disclosures like those in Question #4 are expected to occur within the next 12 months, please provide the anticipated date, type of information to be disclosed, and purpose of the disclosure:

NONE [ ]

This invention would be most useful for ETEC to meet its technical specifications and commitments at IBM, where an RSB is being evaluated and compared to a competing product. Therefore it would be in Applied Materials' business interests to disclose this invention to IBM as soon as possible, in order to improve the ETEC-RSB product performance and gain a competitive advantage.

Preliminary data shows an improvement in resist local CD uniformity as a result of vacuum treatment. CD uniformity improvement in resist is between zero and 1 nm 3sigma, which is significant.

This invention is expected to be of significant interest to the photomask user community. Thus publication, after patent filing protection of IP, would serve Applied Materials' interests in advertising lithographic patterning capabilities.

6. Describe any other known designs or processes, whether actually implemented or merely proposed in a publication, which could be considered similar to your invention or which constitute the state-of-the-art improved upon by your invention: If described in a publication, attach a copy of same or provide a citation.

No known publications describe anything similar to this invention.

A broad search on the US Patent Office website (USPTO.com) scanning for the phrase "resist AND vacuum AND (semiconductor OR lithography OR photomask)" in claims turned up no previous patent which has any similarity to the invention proposed here. There are no reported applications of vacuum processing which claim or report what we are listing below as a novel and non-obvious feature.

The state-of-the-art electron beam photomask processing sequence is summarized:

1. Photomask is coated with resist, post-<sup>application</sup> exposure baked (PAB), and exposed (electron beam or

laser used for creating a pattern onto the photomask resist).

2. The photomask is post-exposure baked (PEB) and developed, which removes the unpatterned resist from the plate.
3. The photomask is then etched, whereby the resist pattern is transferred into an underlying chrome layer. Additional etching may be required for phase-shift masks (PSM).

7. List each feature of the invention which you consider novel and non-obvious. Describe the advantages of each novel feature in comparison with the state-of-the-art approaches which are most similar to your invention:

**Novel and Non-Obvious Features:**

- 1) Use of a post-develop, pre-etch vacuum processing step to reduce variation in critical dimensions on photomasks. The advantage of such a processing step is of enormous benefit to photomask manufacturers. By reducing variation in critical dimensions, the quality of the photomask is improved.

State of the art: No specific vacuum treatment of photomask. The photomask is simply developed, air exposed (and possibly measured in a CD-SEM to get resist CD information), and then the chrome is etched.

- 2) Use of vacuum to alter the composition and dimensions of resist features on a photomask. By applying a vacuum to a photomask (or wafer) for about 20 minutes, water vapor and solvent are desorbed by the surface of the resist. This may enable surface tension (or other mechanisms not yet studied in complete detail) to minimize roughness on the sidewall of a resist feature, which reduces line edge roughness (LER) and also reduces CD variation. Vacuum processing affects the mean CD by only a few nanometers.

State of the art: One commonly applied means of altering resist dimensions on a photomask (or wafer) is the use of a "descum" oxygen plasma step. This basically burns away a fixed amount of resist, which unfortunately reduces the resist dimensions by at least 30nm, but also may also help to smoothen line edges. Descum treatment is not applicable to small feature lithography, since this step consumes a significant amount of lateral resist.

- 3) Application of vacuum treatment to reduce Line Edge Roughness (LER) on resist lines on a photomask (patterned by either electron beam or laser).

State of the art: Descum (see #3 above).

- 4) Application of vacuum to a photomask plate in a photomask etching chamber in which chamber walls and dome are heated, allowing the resist on the photomask to warm to a temperature between 30 degrees C and 55 degrees C, which enables the desorption from the surface of the resist of water vapor, solvents, and materials absorbed onto the surface from the develop process step and other previous steps. In particular, the Applied Materials Tetra etching system is used for this vacuum treatment. Photomasks are placed into a chamber for 20 minutes of vacuum time, where the 55 degree chamber wall and 70 degree dome radiate heat onto the photomask plate. Longer times do not provide any improvement in desorption. The "curve" of resist change is observed to flatten out at 20 minutes.

- ★ 5) Application of a vacuum treatment to a photomask (or wafer) after electron beam exposure (or laser or other methods of resist exposure) to reduce critical dimension variation.

Preliminary data from delayed removal of a photomask from the RSB electron beam writer has shown that CD uniformity may be slightly improved. A nine-hour delay time was utilized in this preliminary work. Delayed removal places the photomask in vacuum for a longer period, prior to air exposure and immediate Post-Exposure Bake. It is possible to perform this vacuum treatment in a Tetra (Applied Materials photomask etcher) chamber, where the vacuum treatment does not impact the RSB throughput. It is also possible to perform the vacuum treatment in other vacuum chambers.

- 6) Generalization of #1 through 5 to include wafers and other substrates. General application to wafers can improve the quality of lithography in the patterning of wafers. Specifically, this can be applied to all wafer lithographic processes where critical dimension control is required, for all wavelengths of light utilized in wafer lithography (G-line, i-line, KrF, ArF, 157) plus other methods used for patterning resist on wafers, such as e-beam, FIB, X-ray, and EUV. Line edge roughness is reduced, and critical dimension control is improved.

8. Describe the invention, preferably with reference to attached drawings:

The invention consists of an additional processing step in the standard "state of the art" sequence described above in Part 6. This is specifically a vacuum applied to the photomask between Step 2 and Step 3 (as noted above in Part 6). Proper timing of the vacuum allows for desorption of materials from the resist surface. Such desorption is found to slightly decrease the thickness of the resist layer. In addition, a slight shrinkage of pattern dimension is observed in the lateral (photomask plane) directions. Moreover, our data shows an improvement in Local CD Uniformity, in which crosses of a given fixed size are printed within a 1mm square, and then measured. Variations in local CD Uniformity can be attributed to a) various electron beam fluctuations during resist patterning and b) process-related line-edge roughness. The ETEC process has succeeded in drastically reducing the latter by creating a proprietary resist and fine-tuning all of the resist-related processing parameters. However, we believe at this time that vacuum processing is capable of further reduction in line-edge roughness, resulting in reduced Local CD Uniformity.

★ Two types of vacuum treatment are described above in the previous section. Vacuum treatment can be applied to a photomask immediately after exposure and before PEB (Post Exposure Bake). This enables acids within the resist to diffuse in such a way as to improve contrast and to reduce line edge roughness.

Another vacuum treatment is applied to the photo mask after develop. In this second vacuum treatment, water vapor and solvents are desorbed from the surface of the patterned resist. In this case, the surface includes sidewalls and the top resist surface. By desorbing the volatile components, the resist loses material and that part of resist close to the surface is in tension. This surface tension may allow for the "pulling together" of the surface which may smooth out sidewall roughness. Since the tension does not apply to the bulk of the resist (deeper than within a few nanometers of the surface), lines and other features are not distorted.

ATTACH ADDITIONAL SHEETS TO DESCRIBE INVENTION AS NEEDED

Provide the following information for EACH inventor\*\* REQUIRED FIELDS:

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10. Signature, date and **PRINTED** name of each inventor plus two witnesses who have read and understood this Invention Alert form:

**Inventors:**

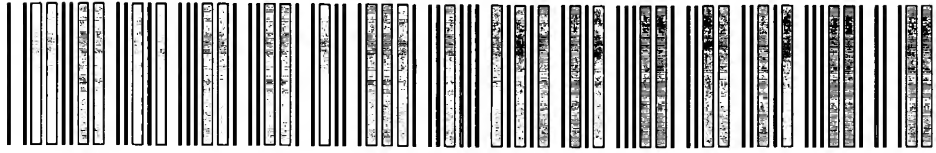
<u>MARK MUELLER</u>	<u>12/17/03</u>	<u>Mark Mueller</u>
Printed Name	Date	Signature
<u>Robert Dean</u>	<u>12/17/03</u>	<u>[Signature]</u>
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<u>K. Ho BATIC</u>	<u>12/17/03</u>	<u>[Signature]</u>
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_____	_____	_____
Printed Name	Date	Signature

**Witness:**

<u>DAMON M. COLE</u>	<u>12/18/03</u>	<u>Damon M. Cole</u>
Printed Name	Date	Signature
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